NEX53100-Q100

Dual-port USB Type-C and Power Delivery controller

Rev. 1 — 25 July 2025 Product data sheet

1. General description

The NEX53100-Q100 is a dual-port USB Type-C and Power Delivery (PD) controller with support for USB D+/D- based fast charging protocols for automotive USB charging applications. It is designed to support Type-C Configuration Channel (CC) detection, PD communication with cables and PD devices, as well as D+/D- power contract negotiation with flash charging supported mobile devices. The connector pins are high-voltage-tolerant to stand against overvoltage or short-circuit conditions.

Dynamic power distribution control, thermal sensing, and input voltage monitoring are implemented to achieve maximum system power and at the same time protect the system from overtemperature or prevent the battery from over-discharge.

I²C master interface is available to support different DC-DC converters.

The NEX53100-Q100 implements high-accuracy detection and control with 10-bit ADC and 8-bit DAC for system monitoring and flexible protections.

2. Features and benefits

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1 (T_{amb}): -40 °C to 125 °C
  - Junction temperature (T_j): -40 °C to 150 °C
- V_{VIN} range: 3.6 V to 24 V (40 V transient)
- USB Type-C and Power Delivery (PD) controller
  - Programmable Type-C default/1.5 A/3 A source current capability advertisement
  - USB PD 3.2 Standard Power Range (SPR) with Programmable Power Supply (PPS), and Adjustable Voltage Supply (AVS)
  - Extended Power Range (EPR) with AVS EPR 28 V support by default, 36 V, 48 V supported with external circuits
  - V_{CONN} power switch integrated
  - SOP' communication support for e-marker
- Other mobile charging protocols
  - Legacy charging protocols
  - UFCS support
  - Proprietary charging protocols
- Wide V_{VBUS} operating range support up to 36 V
- VBUS_Px/CC1_Px/CC2_Px /DP_Px /DM_Px pins with 40 V tolerance to stand against short-to-VBAT or short-to-VBUS
- Programmable GPIOs
- I²C interface as a master interface with internal pull-high to minimize the number of external components
- V_{VBUS} discharge integrates with max 100 mA capability
- Low-power mode support
- Dual external Negative Temperature Coefficient (NTC) thermistors supported with programmable thresholds
- Programmable fault protection and thresholds
  - Adaptive OVP and UVP for VBUS
  - OVP for CC pins and D+/D- pins
  - OTP, supports 2 external NTC thermistors
- Power sharing and load shedding
- MCU and memory
  - Embedded MCU
  - Integrated RAM and Multiple-Time Programmable (MTP)-ROM with Error Correction Code (ECC)
- Available in 4.0 mm x 4.0 mm HWQFN-24 with side-wettable flanks

3. Applications

- Automotive USB charging
- Multi-port power adapters
- Multi-port power storage and power banks

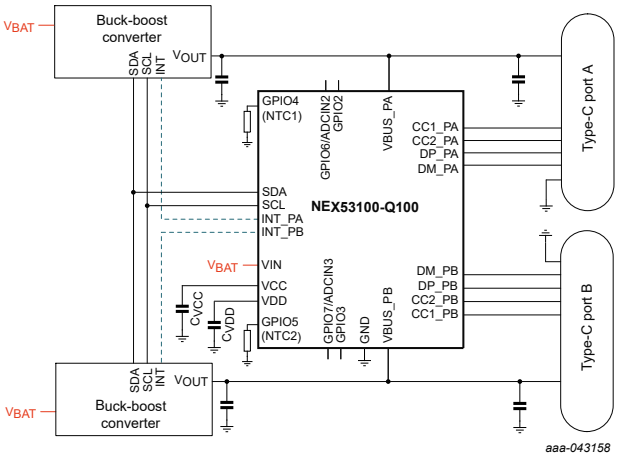


Fig. 1. Typical application diagram

4. Ordering information

Table 1. Ordering information

Type number[1]	Temperature range	Name	Description	Version
NEX5310000BY-Q100	T_{amb} = -40 °C to 125 °C	HWQFN24	plastic thermal enhanced very very thin quad flat package with side-wettable flanks; no leads; 24 terminals; 0.5 mm pitch; 4.0 mm × 4.0 mm × 0.75 mm body	SOT8041D-1

[1] NEX5310000BY-Q100 is shipped with blank memory. The IC needs to be programed with firmware to work. Nexperia offers compensated firmware programming service before shipping the IC with a different type number and top marking under the NEX53100BY-Q100 series.

5. Marking

Table 2. Marking code

Type number	Marking code
NEX5310000BY-Q100	53100 00

6. Pin configuration and description

6.1. Pin configuration

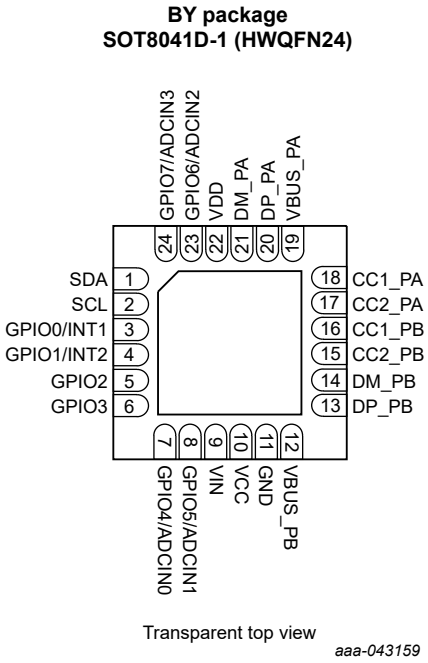


Fig. 2. NEX53100-Q100 (SOT8041D-1/HWQFN24) pin diagram

6.2. Pin description

Table 3. NEX53100-Q100 (SOT8041D-1/HWQFN24) pin description

Symbol	Pin	I/O	Description
SDA	1	I/O	SDA pin for the I²C interface as master; open-drain, can be configured with external pull-high or internally pulled to internal 3.3 V LDO
SCL	2	I/O	SDA pin for the I²C interface as master; open-drain, can be configured with external pull-high or internally pulled to internal 3.3 V LDO
GPIO0/INT1	3	I/O	GPIO0, or could be configured as INT pin from DC-DC for the port A; open-drain, can be configured with external pull-high or internally pulled to internal 3.3 V LDO
GPIO1/INT2	4	I/O	GPIO1, or could be configured as INT pin from DC-DC for the port B; open-drain, can be configured with external pull-high or internally pulled to internal 3.3 V LDO
GPIO2	5	I/O	GPIO2, high-voltage tolerant
GPIO3	6	I/O	GPIO3, HV-tolerant
GPIO4/ADCIN0	7	Analog I/O	GPIO4, or could be configured as ADCIN0 for NTC sensing and IMON input from DC-DC converter for power distribution control
GPIO5/ADCIN1	8	Analog I/O	GPIO5, or could be configured as ADCIN1 for NTC sensing and IMON input from DC-DC converter for power distribution control
VIN	9	PWR	the input power supply to the IC
VCC	10	PWR	output of internal LDO powered from VIN; Connect to capacitor to GND

Symbol	Pin	I/O	Description
GND	11	PWR	ground pin of the IC
VBUS_PB	12	Analog I	VBUS sensing pin, and internal discharge path of VBUS for port B
DP_PB	13	I/O	USB D+ channel for port B
DM_PB	14	I/O	USB D- channel for port B
CC2_PB	15	I/O	Type-C Configuration Channel 2 (CC2) of port B
CC1_PB	16	I/O	Type-C Configuration Channel 1 (CC1) of port B
CC2_PA	17	I/O	Type-C Configuration Channel 2 (CC2) of port A
CC1_PA	18	I/O	Type-C Configuration Channel 1 (CC1) of port A
VBUS_PA	19	Analog I	VBUS sensing pin, and internal discharge path of VBUS for port A
DP_PA	20	I/O	USB D+ channel for port A
DM_PA	21	I/O	USB D- channel for port A
VDD	22	PWR	output of internal LDO; connect to capacitor to GND
GPIO6/ADCIN2	23	Analog I/O	GPIO6, or could be configured as ADCIN2 for NTC sensing and IMON input from DC-DC converter for power distribution control
GPIO7/ADCIN3	24	Analog I/O	GPIO7, or could be configured as ADCIN3 for NTC sensing and IMON input from DC-DC converter for power distribution control
PowerPad	25	PWR	thermal pad, connect PowerPad to PCB ground together with pin 11 (GND)

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter		Conditions	Min	Max	Unit
V_{PIN}	pin voltage	VIN		-0.3	40	V
		VBUS_PA, VBUS_PB		-0.3	40	V
		CC1_PA, CC2_PA, CC1_PB, CC2_PB, DP_PA, DM_PA, DP_PB, DM_PB		-0.3	40	V
		GPIO2, GPIO3		-0.3	40	V
		VCC		-0.3	6	V
		VDD		-0.3	2	V
		SDA, SCL, GPIO0, GPIO1		-0.3	6	V
		GPIO4 to GPIO7		-0.3	6	V
I_{OUT}	output current	source current on CC1_PA, CC2_PA, CC1_PB, CC2_PB	with consideration of CC pins acting as V_{CONN}	-	100	mA
		GPIO2 to GPIO7		-	5	mA
		SDA, SCL, GPIO0, 1	open-drain output	-	10	mA
		DP_PA, DM_PA, DP_PB, DM_PB		-	10	mA
T_{amb}	operating ambient temperature			-40	125	°C
T_j	operating junction temperature			-40	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Stresses beyond those conditions under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 3B	[1][2]	-8000	-	8000	V
		HBM: ANSI/ESDA/JEDEC JS-001 class 3A	[1][3]	-4000	-	4000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3	[4]	-2000	-	2000	V

[1] HBM stressing is in accordance with AEC-Q100-002.
[2] Pin CC1_PA, CC2_PA, CC1_PB, CC2_PB, DP_PA, DM_PA, DP_PB, DM_PB, VBUS_PA, VBUS_PB, GPIO2, GPIO3.
[3] Pin VDD, GPIO6/ADCIN2, GPI07/ADCIN3, SDA, SCL, GPIO0/INT1, GPIO1/INT2, GPIO4/ADCIN0, GPIO5/ADCIN1, VIN, VCC, GND.
[4] CDM stressing is in accordance with AEC-Q100-011.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Typical values correspond to T_j = 25 °C. Minimum and maximum limits apply over -40 °C to 125 °C ambient temperature range unless otherwise stated. VCC = 5 V for the recommended operating conditions unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VIN}	supply voltage		3.6[1]	-	24[2]	V
V_{VBUS}	VBUS operation voltage		0	-	36	V
	VBUS expected input voltage range (to cover whole PPS range)		3.3	-	21[3]	V
	VBUS effective operation & sensing range		3	-	36	V
$V_{I/O}$	GPIO2/GPIO3		0	-	36	V
	CC1_PA, CC2_PA, CC1_PB, CC2_PB		0	-	5.5	V
	DP_PA, DM_PA, DP_PB, DM_PB		0	-	5.5	V
	SDA, SCL, GPIO0, GPIO1		0	-	5.5	V
	GPIO4 to GPIO7		0	-	5.5	V
$I_{I/O}$	CC1_PA, CC2_PA, CC1_PB, CC2_PB		-	-	20	mA
	DP_PA, DM_PA, DP_PB, DM_PB		-	-	10	mA
C_{VBUS}	effective VBUS capacitance		-	-	3000[4]	µF
C_{VCC}	capacitance on VCC		1.0[5]	2.2	4.7	µF
C_{VDD}	capacitance on VDD		1.0[5]	2.2	4.7	µF
T_{amb}	operating ambient temperature		-40	-	125	°C
T_j	operating junction temperature		-40	-	150	°C

[1] A minimum of 5 V operating V_{VIN} is recommended for IC fully functioning consideration. Operation with V_{VIN} < 5 V is designed to support cold-cranking or transient battery voltage drop operations but not recommended as normal operation voltage. The I/O output capability, Type-C advertisement and detection functions will be partially limited for V_{VIN} lower than 5 V.
[2] V_{VIN} > 24 V operation can be supported in transient conditions but not supported as continuous operating voltage. V_{VIN} > 40 V may lead to device damage.
[3] PD 3.2 EPR 36 V/48 V could be supported by adding an extra resistor divider.
[4] 3000 µF maximum is defined in Type-C specification for V_{VBUS} when Type-C acts as the source role only.
[5] Requires effective capacitance to be minimum 1 µF to ensure reliable operation of the device.

10. Thermal information

Table 7. Thermal information

Symbol	Parameter	SOT8041D-1 (HWQFN-24)	Unit
$R_{\theta JA}$	junction to ambient thermal resistance	45.87	°C/W
$R_{\theta JC(top)}$	junction to case (top) thermal resistance	42.35	°C/W
$R_{\theta JB}$	junction to board thermal resistance	24.42	°C/W
Φ_{JT}	junction to top char parameter	8.53	°C/W

11. Electrical characteristics

Power supply characteristics

Table 8. Power supply parameters

Typical values correspond to T_j = 25 °C. Minimum and maximum limits apply over -40 °C to 125 °C ambient temperature range unless otherwise stated. VCC = 5 V (V_{VIN} > 5.5 V) unless otherwise stated.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
V_{VIN}	supply voltage		3.6	-	24.0	V
V_{VCC_POR}	VCC threshold for POR	V_{VIN} rising	3.0	3.3	3.6	V
V_{VCC_UVLO}	VCC threshold as UVLO	V_{VIN} falling	2.3	2.5	2.7	V
VCC	output of internal LDO	V_{VIN} = 2.7 V to 3.6 V [1]	V_{VIN} - 0.5	-	V_{VIN}	V
		V_{VIN} = 3.6 V to 5.5 V [2]	V_{VIN} - 0.5	-	V_{VIN}	V
		V_{VIN} = 5.5 V to 36.0 V [3]	4.5	5.0	5.5	V
VDD	output of internal LDO		1.35	1.50	1.65	V
I_{act}	all block active	not counting in V_{CONN} consumed current average power consumption, no protocol communication and I²C transaction	-	5	-	mA
I_{lp}	low-power mode current	V_{VIN} = 12 V or VCC = 5 V; no connection; pull-high power and connection detection comparators are enabled to wake up the IC	-	150	-	µA

[1] MCU power is alive to monitor the IC and response. Connection reset may happen.
[2] If the connection exists, maintain the connection status. V_{CONN} switch may shut down if V_{CONN} voltage drops < 3 V. MCU is alive to monitor the IC status. Expected in cold cranking (consider 65 ms maximum).
[3] Normal voltage range; the IC is fully functioning.

VBUS sensing protections and alerts

Table 9. VBUS parameters

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
I_{VBUS_DCHG}	VBUS discharge current		-	100	-	mA
VBUS_OVP	programmable rising threshold to trigger VBUS OVP percentage of the maximum negotiated voltage		disabled			-
			-	10	-	%
			-	15	-	%
			-	20	-	%
VBUS_UVP	programmable falling threshold to trigger VBUS UVP		-	-15	-	%
			-	-20	-	%
			-	-25	-	%
			-	-30	-	%
VBUS_SC	VBUS short-circuit detection threshold	equivalent as percentage of VBUS	-	-50	-	%
$T_{VBUS\_OVUV\_BLK}$	blanking time after VBUS OV or UV protection		-	200	-	ms

CC detection and PD PHY characteristics

Table 10. CC and PD physical layer information

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
CC1/2 detection parameters (Type-C function)						
$I_{Rp\_default}$	Type-C source current at default current		64	80	96	µA
$I_{Rp\_1.5A}$	Type-C source current at 1.5 A		166	180	194	µA
I_{Rp_3A}	Type-C source current at 3 A		304	330	356	µA
$t_{CC\_deglitch}$	deglitch time for CC1/CC2 comparators		-	3.2	-	ms

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
V_{th_Rd}	threshold for internal circuit to start CC recognition for R_d when configured to default or 1.5 A Type-C source current	falling	-	1.6	-	V
	threshold to detect the disconnection on default or 1.5 A configuration	rising	-	1.65	-	V
	hysteresis		-	0.05	-	V
	threshold for internal circuit to start CC recognition for R_d when configured to 3 A Type-C source current	falling	-	2.65	-	V
	threshold to detect the disconnection on 3 A configuration	rising	-	2.75	-	V
	hysteresis		-	0.1	-	V
V_{th_Ra}	threshold for internal circuit to start CC recognition for R_d when configured to default Type-C source current	falling	0.2	-	-	V
	threshold for internal circuit to start CC recognition for R_d when configured to 1.5 A Type-C source current	falling	0.4	-	-	V
	threshold for internal circuit to start CC recognition for R_d when configured to 3 A Type-C source current	falling	0.8	-	-	V
R_{CC_OPEN}	resistance from CC to GND in CC open state		1000	-	-	kΩ
V_{CC_OVP}	CC pin OVP threshold		-	5.75	-	V
V_{CC_OL}	open loop voltage for CC1 or CC2		-	3.3	-	V
CC-V_{CONN} parameters						
V_{CONN_valid}	V_{CONN} output voltage range		3	VCC	5.5	V
I_{VCONN}	source current capability on V_{CONN}		20	-	-	mA
I_{VCONN_OCP}	overcurrent detection threshold		-	30	-	mA
I_{VCONN_short}	V_{CONN} short circuit protection threshold		-	70	100	mA
$t_{VCONN\_OCP\_deglitch}$	deglitch time to trigger V_{CONN} OCP		-	1.28	-	ms
t_{VCONN_SC}	response time for V_{CONN} short circuit		-	-	0.5	µs

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
I_{CC_LKG}	leakage current into CC pins, maximum for current flow into the connector side, the minimum indicates that the current flows into VCC	V_{CONN} disabled; VCC or CC pin voltage = 5 V; measure current	-2	-	2	µA
$R_{DS(on)\_VCONN}$	V_{CONN} switch $R_{DS(on)}$		-	10	20	Ω
$V_{VCONNdischarge}$	V_{CONN} voltage expected after $t_{VCONNdischarge}$		-	-	800	mV
$t_{VCONNdischarge}$	time from cable disconnection to V_{CONN} drop below 800 mV		-	-	230	ms
t_{VCONN_ON}	time for V_{CONN} reach 3 V after V_{VBUS} reach vSafe 5 V, or after executing V_{CONN} swap to be a V_{CONN} source		-	-	2	ms
t_{VCONN_OFF}	when successfully executes V_{CONN} swap, or after state detection of a disconnection		-	-	35	ms
BMC common parameters						
$f_{bitrate}$	bit rate		270	300	330	kbps
$t_{unitinterval}$	bit unit interval	$1/f_{BitRate}$	3.03	3.30	3.70	µs
BMC transmitter parameters						
$p_{bitrate}$	maximum difference between the bitrate during the part of the packet following the preamble and the reference bitrate.	the reference bit rate is the average bit rate of the last 32 bits of the preamble	-	-	0.25	%
$t_{enddriveBMC}$	time to cease driving the line after the end of the last bit of the frame	minimum value is limited by $t_{holdlowBMC}$	-	-	23	µs
$t_{holdlowBMC}$	time to cease driving the line after the final high-to-low transition	maximum value is limited by $t_{enddriveBMC}$	1	-	-	µs
$t_{interframegap}$	time from the end of last bit of a frame until the start of the first bit of the next preamble		25	-	-	µs
$t_{startdrive}$	time before the start of the first bit of the preamble when the transmitter shall start driving the line		-1	-	1	µs
$V_{TX\_CC\_H}$	Biphase Mark Coding (BMC) transmitter high voltage	applies to both no load condition and under the load condition specified in CC1/2 transmitter load mode	1.050	1.125	1.200	V

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
$V_{TX\_CC\_L}$	BMC transmitter low voltage	applies to both no load condition and under the load condition specified in CC1/2 transmitter load mode	-75	-	75	mV
t_{BMC_rise}	BMC rising time	R_{load} = 5.1 kΩ; C_{load} = 1 nF; C_{cc} = 520 pF; 10% and 90% amplitude points, minimum is under an unloaded condition of CC1/CC2	300	-	-	ns
t_{BMC_fall}	BMC falling time		300	-	-	ns
$Z_{BMCdriver}$	transmitter output impedance	during transmission	33	50	75	Ω
BMC receiver parameters						
$C_{receiver}$	CC receiver capacitance	DFP system shall have capacitance within this range when not transmitting on the line	200	-	600	pF
n_{BER}	bit error rate, S/N = 25 dB		-	-	10^{-6}	-
$n_{transitioncount}$	transitions for signal detect	number of transitions to be detected to declare bus non-idle	3	-	-	-
$t_{Rxfilter}$	Rx bandwidth limiting filter (digital or analog)		100	-	-	ns
$t_{transitionwindow}$	time window for detecting non-idle		12	-	20	µs
$V_{noiseactive}$	noise amplitude when BMC is active		-	-	165	mV
$V_{noiseidle}$	noise amplitude when BMC is idle		-	-	300	mV
Z_{BMCRx}	receiver input impedance	does not include pull-up or pull-down resistance from cable detect transmitter is Hi-Z	1	-	-	MΩ

D+/D- detection PHY characteristics

Table 11. D+/D- interface information

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
BC 1.2 interface parameters						
t_{DBC_H}	D+, D- high debounce time		1.0	-	1.5	s
t_{DBC_DISC}	D+ disconnect debounce time		40	-	-	ms
R_{DCP_DAT}	D+ to D- short resistance during DCP mode		-	20	40	Ω
V_{DP_CD}	D+ comparison threshold for cable detection		0.250	0.325	0.400	V
D+/D- OVP parameters						

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
V_{DP_OVP}	D+ OVP threshold		-	5.75	-	V
			-	4.75	-	V
V_{DM_OVP}	D- OVP threshold		-	5.75	-	V
			-	4.75	-	V

Thermal sensing characteristics

Table 12. Thermal sensing parameters

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
Thermal protection						
T_{SD}	thermal shutdown temperature	rising junction temperature	160	-	175	°C
	thermal shutdown hysteresis		-	20	-	°C
T_{NTC_IN}	internal temperature sensing range		-40	-	160	°C
T_{NTC_T}	tolerance for NTC sensing		-10	-	10	°C
V_{NTC}	NTC open loop voltage		-	3.3	-	V
V_{NTC_EXT}	external temperature sensing range	depends on NTC thermistor selection; reflects into ADC input sensing range	0	-	VCC	V
I_{NTC_EXT}	external NTC pull-high current	pull-high applied on GPIO4 (PIN7), GPIO5 (PIN8) thermistor will be suggested as 47 kΩ or 100 kΩ	disabled			-
			-	4	-	µA
			-	37	-	µA
			-	100	-	µA

I/O characteristics

Table 13. I/O parameters

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
I/O configured as outputs						
V_{OH}	GPIO high level output voltage	GPIO open voltage for logic high and logic low	3.0	3.3	3.6	V
V_{OL}	GPIO low level output voltage		-	-	0.4	V
I_{OH1}	GPIO push-pull high-level current	GPIO0, 1, 2, 3, 4, 7; equivalent to internal pull-up with 2.8 kΩ resistor	-	1	2	mA
I_{OH2}	GPIO push-pull high-level current	GPIO5, 6	-	2	-	mA
I_{OL}	GPIO pull-low capability	GPIO0 to GPIO1, GPIO4 to GPIO7	-	5	-	mA
I_{OL}	GPIO pull-low capability	GPIO2 to GPIO3	-	1	-	mA
I/O configured as inputs						

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
V_{IH}	GPIO high level input voltage		1.3	-	-	V
V_{IL}	GPIO low level input voltage		-	-	0.54	V
I_{IO_LKG}	GPIO leakage	V_{GPIO} = 5 V	-10	-	10	µA
R_{IO_PU}	GPIO internal pull-up resistance	when internal pull-up enabled	-	2.8	-	kΩ

I²C characteristics

Table 14. I²C parameters

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
SDA and SCL parameters (standard and fast mode)						
V_{IH}	GPIO high level output voltage		1.3	-	-	V
V_{IL}	GPIO low level output voltage		-	-	0.54	V
SDA and SCL parameters, standard mode						
f_{SCLS}	clock frequency		-	-	100	kHz
$t_{HD;STA}$	start or repeated start condition hold time		4	-	-	µs
t_{LOW}	SCL clock low time		4.7	-	-	µs
t_{HIGH}	SCL clock high time		4	-	-	µs
$t_{SU;STA}$	start or repeated start condition setup time		4.7	-	-	µs
$t_{HD;DAT}$	serial data hold time		0	-	-	ns
$t_{SU;DAT}$	serial data setup time		250	-	-	ns
t_r	rise time of SCL and SDA signals	R_{PU} = 2.8 kΩ; C_b = 200 pF; measure rising from 0.3 to 0.7	-	-	1000	ns
t_{of}	output fall time from VIH (MIN) to VIL (MAX)	measure rising from 0.3 to 0.7	-	-	250	ns
t_f	fall time of SCL and SDA signals	3.3 V; R_{PU} = 2.8 kΩ; 10 pF < C_b < 200 pF	-	-	300	ns
$t_{SU;STO}$	stop condition setup time		4	-	-	µs
t_{BUF}	bus free time between stop and start		4.7	-	-	µs
$t_{VD;DAT}$	valid data time	SCL low to SDA output valid	-	-	3.45	µs
$t_{VD;ACK}$	valid data time of ACK condition	ACK signal from SCL low to SDA valid	-	-	3.45	µs
SDA and SCL parameters, fast mode						
f_{SCLS}	clock frequency		-	-	400	kHz
$t_{HD;STA}$	start or repeated start condition hold time		0.6	-	-	µs

Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ	Max	
t_{LOW}	SCL clock low time		1.3	-	-	µs
t_{HIGH}	SCL clock high time		0.6	-	-	µs
$t_{SU;STA}$	start or repeated start condition setup time		0.6	-	-	µs
$t_{HD;DAT}$	serial data hold time		0	-	-	ns
$t_{SU;DAT}$	serial data setup time		100	-	-	ns
t_r	rise time of SCL and SDA signals	R_{PU} = 2.8 kΩ; C_b = 200 pF; measure rising from 0.3 to 0.7	20	-	300	ns
t_{of}	output fall time from VIH (MIN) to VIL (MAX)	3.3 V; measure rising from 0.3 to 0.7	12	-	250	ns
t_f	fall time of SCL and SDA signals	3.3 V; R_{PU} = 2.8 kΩ; 10 pF < C_b < 200 pF	12	-	300	ns
$t_{SU;STO}$	stop condition setup time		0.6	-	-	µs
t_{BUF}	bus free time between stop and start		1.3	-	-	µs
$t_{VD;DAT}$	valid data time	SCL low to SDA output valid	-	-	0.9	µs
$t_{VD;ACK}$	valid data time of ACK condition	ACK signal from SCL low to SDA valid	-	-	0.9	µs

12. Detailed description

The NEX53100-Q100 is a USB Type-C and Power Delivery (PD) controller with support to multiple D+/D- based fast charge protocols. It is designed for the automotive USB charging interface in power source application supporting Type-C CC detection, PD communication with cables and PD devices, as well as D+/D- power contract negotiation with flash charging supported mobile devices.

I²C interface is supported at the same time to work with different DC-DC converters.

The NEX53100-Q100 implements high-accuracy detection and control with 10-bit ADC.

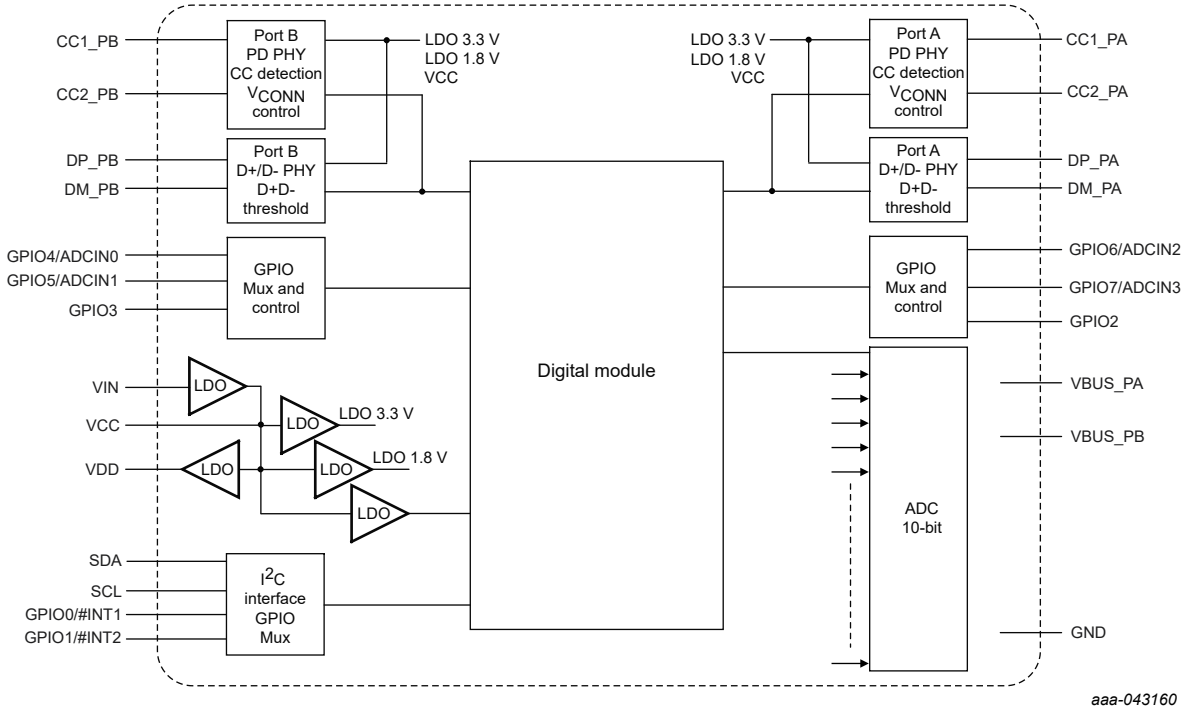


Fig. 3. NEX53100-Q100 functional block diagram

12.1. USB Type-C and PD

Features

- Programmable Type-C default, 1.5 A, 3 A source capability advertisement
- USB PD 3.2 compliant, support up to 11 PDOs
  - SPR with PPS and AVS
    - Fixed PDO – source: 5 V, 9 V, 15 V, 20 V at 5 A max
    - APDO: PPS range of 5 V to 11 V, 5 V to 16 V, 5 V to 21 V at 3 A max, and 3.3 V to 21 V at 5 A max; AVS range of 9 V to 15 V/15 V to 20 V at 5 A max
  - EPR with AVS
    - Fixed PDO, 28 V, 36 V, 48 V at 5 A max
    - APDO: 15 V to 28 V, 15 V to 36 V, 15 V to 48 V at 5 A max
- V_{CONN} power supply and switch integrated; the PD controller supports V_{CONN}
- SOP' communication support for e-marker; supports SOP' packet type to communicate with e-makers

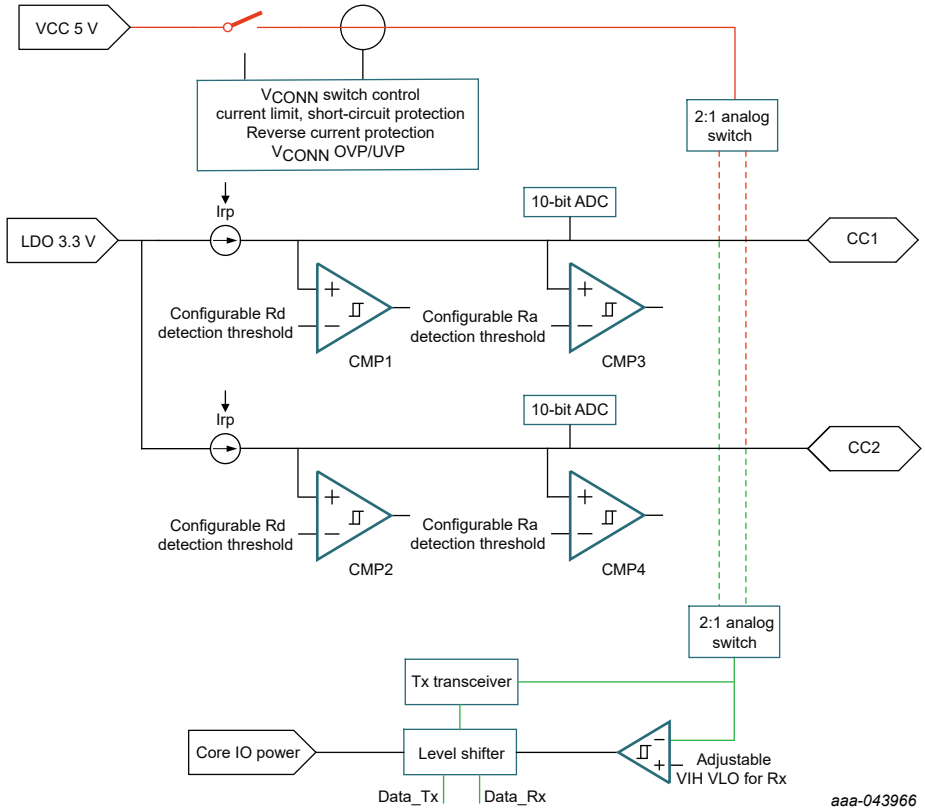


Fig. 4. Type-C and PD physical layer block diagram

12.2. D+/D- interface

The NEX53100-Q100 supports BC 1.2 DCP by default for dedicated charging applications. At the same time, in order to support the data connection through D+ and D- wires in some applications, the NEX53100-Q100 also supports CDP operation. Note that the data lines will be released to data communication after CDP detections, enabling of CDP mode will lead to the abandonment of D+/D- based proprietary protocols.

12.3. I²C, GPIO functionality and ADC configurations

The NEX53100-Q100 is designed with 8 GPIOs, together with an I²C interface.

12.3.1. I²C functions

The NEX53100-Q100 integrates one I²C interface that can work as Master that proactively controls the DC-DC converters, polling the status registers or response to the I²C interrupts usually in response of the fault alerts from the DC-DC converters.

At the same time, the same I²C interface is standby as a slave interface and can be activated as an I²C slave through a key code to work as a firmware programing interface.

12.3.2. GPIO configurations

Table 15 lists the configurations of each IO.

Table 15. GPIO configurations

PIN/Channel	INT	Internal pull-up	Open-drain output	Push-pull output	Digital input	Analog input (ADC)	Special function
SDA		√	√				
SCL		√	√				
GPIO0	√	√	√	√	√		INTx_PA
GPIO1	√	√	√	√	√		INTx_PB
GPIO2[1]		√	√	√	√	√[1]	Liquid detection input
GPIO3[1]		√	√	√	√	√[1]	Liquid detection input
GPIO4		√	√	√	√	√	NTC with current source
GPIO5		√	√	√	√	√	NTC with current source
GPIO6[1]		√		√	√	√	
GPIO7[1]		√		√	√	√	

[1] Refer to Section 12.8 for more details. GPIO2 and GPIO3 occupy the ADCIN channels of GPIO6 and GPIO7 respectively when liquid detection function is enabled on the two pins.

12.3.3. ADC channel divider ratios and peak sensing range

ADC channels are enabled as analog input channels to detect external signals. The internal reference value is typically at 2.046 V. The internal divider ratios, peak sensing range, and corresponding pin voltage tolerance are described in Table 16.

Table 16. Channels, divider ratios and peak sensing range

ADC channel	Divider ratio	Sensing range	Pin max input voltage
ADCIN0	1	2.046 V	5.5 V
ADCIN1	1	2.046 V	5.5 V
ADCIN2	1	2.046 V	5.5 V
ADCIN3	1	2.046 V	5.5 V
CC1_PA / CC1_PB	1/5	10.23 V	36 V
CC2_PA / CC2_PB	1/5	10.23 V	36 V
DP_PA / DP_PB	1/4	8.184 V	36 V
DM_PA / DM_PB	1/4	8.184 V	36 V
VBUS_PA / VBUS_PB	FW selectable 1/10	20.46 V	36 V
	1/20	40.92 V	
VIN	1/20	-	24 V

12.4. VBUS discharge

The NEX53100-Q100 is designed with integrated discharge circuit to support configurable discharge current through VBUS pins. The VBUS discharge function benefits the system design to assure voltage-dropping transitions compliant to the USB Type-C and USB PD regulations.

12.5. Power modes

The NEX53100-Q100 is designed with low-power mode to minimize power consumption.

12.5.1. Active mode (output active, all function block active)

Active mode indicates the device is fully-functioning with all the function blocks active in power-on mode to be activated for operation.

12.5.2. Low-power mode (no connection)

Low-power mode is designed to minimize system power consumption in the non-connection state.

After configurable delay upon connection removal or after the PoR, the device will enter LPM if the function is enabled. A connection status change (Rd or Ra detected for a Type-C connection, or 0.325 V D+ detection threshold is triggered for a legacy or proprietary protocol connection) will trigger the IC to resume active mode operation.

12.6. External thermal sensing and protection

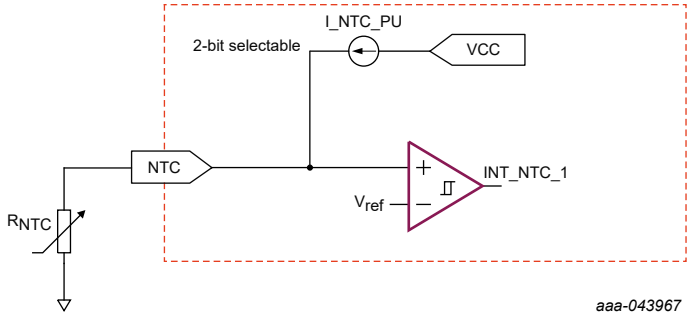


Fig. 5. Block diagram of external NTC sensing

The NTC feature allows to connect the NTC GPIO to the external thermal resistors to implement thermal protection or alert functions. The NEX53100-Q100 supports up to 2 NTCs with 3 steps of selectable source current so that the thermistor can be directly connected to the GPIO pins for the thermal sensing functions. Note that the internal current source is only available on GPIO4 and GPIO5.

12.7. Dynamic system power management

The dynamic power management feature supports a timely adjustment of the system output power when the system has over-temperature concerns, or when the battery voltage drops lower than rated.

The power sharing algorithm and load shedding algorithms are implemented through firmware with flexibility to be customized. For example:

- NTC, to tune down/resume system output power when the temperature goes higher/lower than the defined threshold.
- VIN, to tune down/resume system output power when the battery voltage gets lower/higher than the defined threshold.
- IMON or PMON, the dynamic power management may use the real-time power consumption information from the DC-DC converters that can be achieved through its IMON or PMON output pins. The detection can be achieved through the ADCIN pins of NEX53100-Q100.

12.8. Liquid detection

Liquid detection function is implemented to protect the connector pad from electrochemical corrosion.

By using the idle SBU pins or specially designed pins of the Type-C connector, the NEX53100-Q100 can monitor the change of pin impedance so that it can determine if the liquid flows into the Type-C connector. If the liquid is detected in the connector, the NEX53100-Q100 can cut off the VBUS output, or disable CC pull-ups when disconnected.

In consideration of the potential short-to-VBUS fault on the SBU pins, GPIO2 and GPIO3 are equipped with HV isolation and the internal pull-up/downs specifically for the detection function. GPIO6 and GPIO7 ADCIN function will be disabled by default if liquid detection function is enabled.

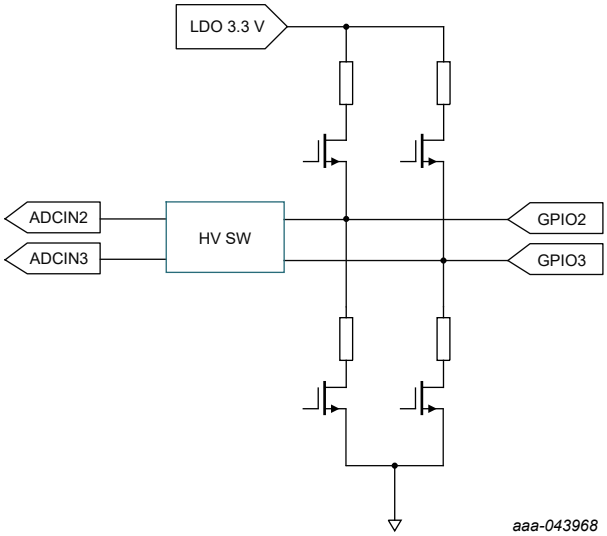


Fig. 6. Internal connection for liquid detection function

12.9. Memory and firmware programming

12.9.1. MTP ROM with ECC

The NEX53100-Q100 integrates RAM and MTP ROM to realize flexible application algorithms. The MTP ROM supports up to 1000 times of programming to ensure that the IC functions across entire end-product design, evaluation, production, and even post-production firmware upgrades.

The error correction code is implemented in NEX53100-Q100 MTP. It can detect and correct single-bit errors and detect (but not correct) more-bit errors. As a result, it assures the data accuracy and provides higher stability and reliability by preventing data corruption and system crash in the long-term operation.

The ECC function is selectable to be enabled and equivalently takes partial of the overall ROM size open for firmware programing.

12.9.2. Bit-lock function

The bit-lock function is designed to protect customers' firmware data against being stolen or improper programmed. The function can be enabled through the firmware. Once enabled, all the readback data from the memory is 0x00 instead of the real values. The bit-lock function is suggested only to be enabled on mass-production product with final-version firmware that not requires further modifications.

12.9.3. Firmware programming and update

The NEX53100-Q100 needs to be programmed with proper firmware that is unique with an end-product to work properly.

Firmware programming through I²C interface is available on both fresh IC and programmed IC. The OTA (Over-The-Air) updates is also available through I²C interface after the end-product is released to the market.

At the same time, programing through the Type-C port is reserved to better support development and validation on end products. Note that both CC1 and CC2 are required to program through Type-C and can only work on the programmed IC with the Type-C function enabled. Either of the 2 ports supports the function.

The on-line (OTA) and offline (through Type-C) programing allow flexibility to update the firmware in case of any compatible issue happens, post-production requirements to be compliant with latest protocol upgrades.

Nexperia offers compensated firmware programming services so that the IC can be shipped with firmware also with a specific type number and top-marking. Nexperia also provides a firmware programing guide to I²C when the common part number NEX5310000BY-Q100 with blank firmware is ordered.

12.10. Boundary operation clarifications

12.10.1. Recommended and most favorable operating conditions

A minimum of 5 V operating V_{VIN} is recommended for IC fully functioning considerations. 3.6 V to 24 V assures the IC to support cold-cranking or transient battery voltage drop operations. Note that V_{VIN} < 5 V partially limits the I/O output capability, Type-C advertisement and detection functions, thus it is not recommended as the nominal operation voltage.

The most favorable V_{VIN} range is 5.5 V to 24 V, which allows nominal VCC output at 5 V to support V_{CONN} defined typical voltage, as well as with promised electrical characteristics and power consumption performance.

12.10.2. Load dump operating condition

Load dump transient occurs in the event of a discharged battery being disconnected while the alternator is generating charging current with other loads remaining on the alternator circuit. The target of NEX53100-Q100 is a 12-V system where the supply voltage for the generator is in operation, as well as the test case is defined as U_A to be 13.5 ± 0.5 V as regulated in ISO16750-1 and 14 V in ISO7673-2.

When load dump happens, with proper design of filtering/clamping circuit, the load dump can be suppressed to match with the defined test B (with centralized load dump suppression) as regulated in ISO16750-2.

The NEX53100-Q100 is designed with operating range up to 36 V to fully support such load conditions.

12.10.3. Cold cranking operating condition

Normally, the output of a 12 V vehicle battery can vary from 9 V to 16 V. If a cold-cranking condition happens, the battery voltage can drop down to 3 ± 0.2 V, indicating that 2.8 V is the worst case to be considered, for a duration of 15 ms. Then the battery voltage goes up step by step.

With this condition considered, V_{VCC_UVLO} threshold is defined as 2.7 V (max) so that the IC internal block will remain alive and the MCU can take necessary actions, for example, reset the IC or system if required.

In any case when the VCC drops below V_{VCC_UVLO}, the NEX53100-Q100 powers off and waits for the next power-on reset.

13. Protections

13.1. Overvoltage protection (OVP)/undervoltage protection (UVP)/undervoltage lockout (UVLO) and comparators for VBUS

V_{VBUS} is monitored for internal and external circuits protection and reset.

- VBUS_OVP is 2-bit programmable with 5%, 10%, 15%, 20% thresholds.
- VBUS_UVP is 2-bit programmable with -15%, -20%, -25%, and -30% thresholds.
- UVLO puts the IC into shutdown mode. All internal blocks are powered off.

13.2. Overvoltage protection (OVP) for CC1, CC2 and D+/D-

The D+/D- and CC pins are designed with high voltage tolerance, CC/D+/D- OV is configurable through the firmware.

13.3. Short protection

VBUS - 50% threshold is considered as a V_{VBUS}-short condition and is enabled through the firmware.

13.4. V_{CONN} OVP/UVP/RCP and V_{CONN} current limit (OCP/SCP)

The V_{CONN} switch is bi-directionally blocked when disabled. V_{CONN} OVP/UVP/OCP are implemented and selectable through the firmware. V_{CONN} SCP is designed with quick response to protect the device when CC/V_{CONN} pins are short to GND. RCP is implemented to prevent the current from flowing into the VCC pin.

13.5. Thermal shutdown

The junction temperature (T_j) of the device is monitored by an internal temperature sensor. If the T_j exceeds the thermal shutdown temperature (T_{SD}) above 160 °C, the device enters thermal shutdown. When T_j decreases below the hysteresis level at typically 20 °C, the device resumes functioning.

14. Application and implementation

Application diagram

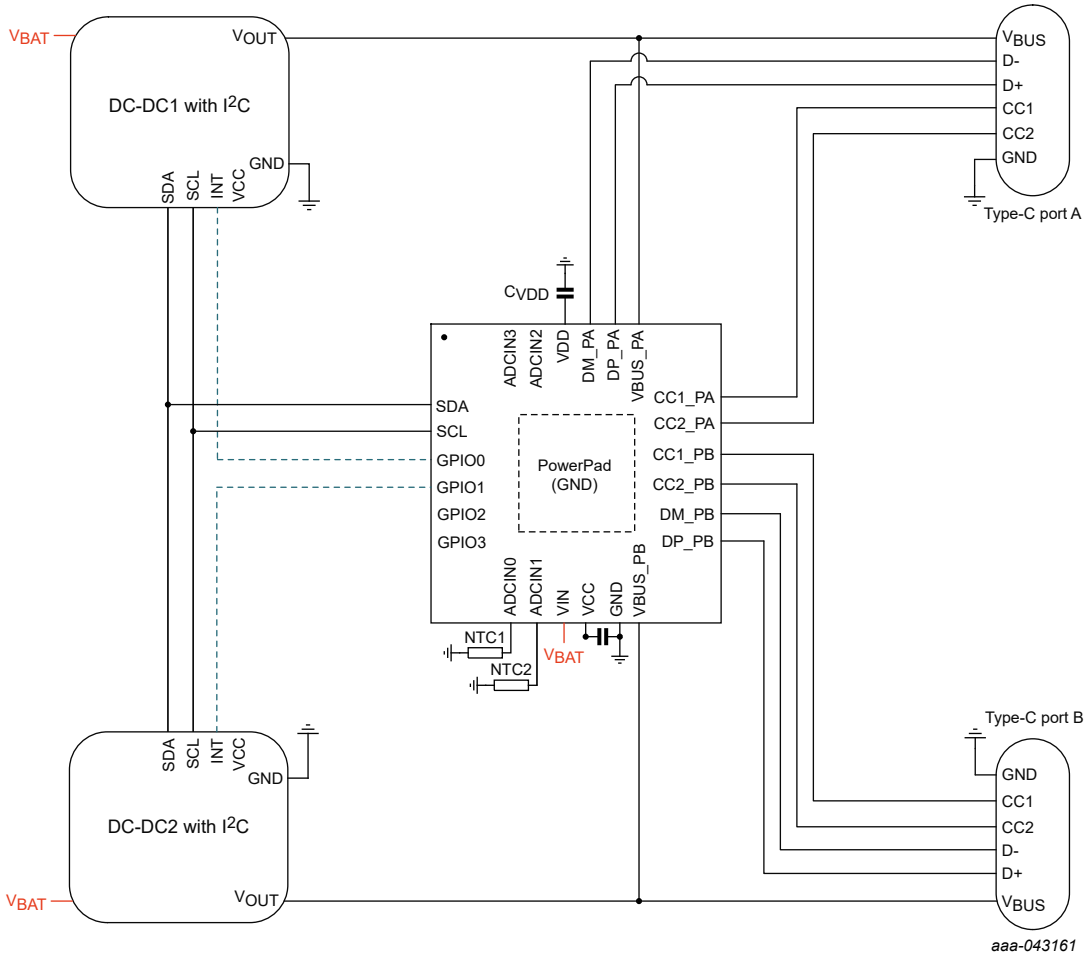


Fig. 7. Typical application block diagram

Table 17. Reference application parameters

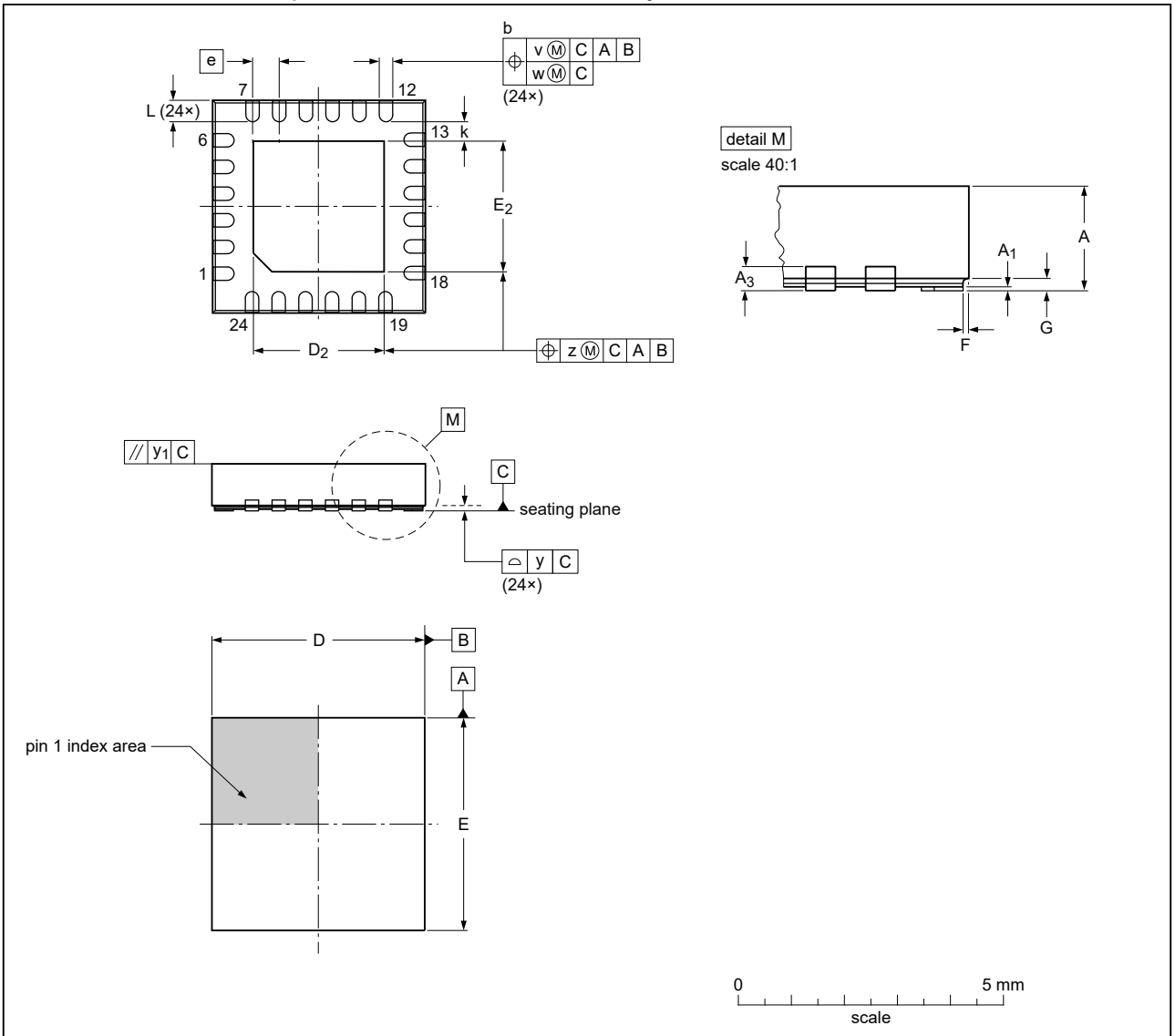
Reference parameters proposed based on system block described in Fig. 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	typical car battery voltage		-	12	-	V
V_{BUS}	VBUS pin voltage range		-	20	28	V
I_{BUS}	output load current	[1]	-	3	5	A
NTC1	NTC thermistor link to port A	[2]	-	100	-	kΩ
NTC2	NTC thermistor link to port B	[2]	-	100	-	kΩ

[1] Determined by DC-DC converter capability and customer specifications.
[2] GPIO4 and GPIO5 are enabled as NTC function with internal pull-up current source. NTC thermistor 100 kΩ at 25 °C; B = 3590 is adopted for the reference block.

15. Package outline

Plastic thermal enhanced very very thin quad flat package with side-wettable flanks; no leads; 24 terminals; 0.5 mm pitch; 4.0 mm × 4.0 mm × 0.75 mm body **SOT8041D-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_3	b	D	D_2	E	E_2	e	F	G	k	L	v	w	y	y_1	z
mm	max	0.80	0.05	0.203 REF	0.30	4.10	2.55	4.10	2.55	0.50 BSC	0.05 REF	0.10	0.375 REF	0.50	0.1	0.05	0.08	0.1	0.1
	nom	0.75			0.25	4.00	2.45	4.00	2.45					0.40					
	min	0.70			0.20	3.90	2.35	3.90	2.35					0.30					

sot8041d-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8041D-1						25-02-10

Fig. 8. Pin configuration SOT8041D-1 (HWQFN24)

16. Abbreviations

Table 18. Abbreviations

Acronym	Description
AC	Alternate Current
APDO	Augmented Power Data Object
AVS	Adjustable Voltage Supply
CC	Configuration Channel
CDM	Charged Device Model
DC	Direct Current
ECC	Error Correction Code
EPR	Extended Power Range
HBM	Human Body Model
LDO	Low-DropOut
MCU	Microcontroller Unit
MTP-ROM	Multi-time Programmable Read-Only Memory
NTC	Negative Temperature Coefficient
OCP	OverCurrent Protection
OTA	Over-The-Air
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PD	Power Delivery
PDO	Power Data Object
PPS	Programmable Power Supply
RAM	Random Access Memory
SPR	Standard Power Range
USB	Universal Serial Bus
UVLO	UnderVoltage LockOut
UVP	UnderVoltage Protection

17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX53100_Q100 v. 1	20250725	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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