RX260/RX261 Group, RX210 Group

Differences Between the RX260/RX261 Group and RX210 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX261 Group and RX210 Group. It also explains key points to consider when migrating between the two groups.

Unless otherwise specifically noted, the information in this application note applies to the 100-pin package version of the RX261 Group and the 145-pin package version of the RX210 Group as the maximum specifications. For details about the differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual of the products in question.

Target Devices

- RX260/RX261 Group, RX210 Group

Contents

1. Comparison of Built-In Functions of RX260/RX261 Group and RX210 Group

The following is a comparison of the built-in functions of the RX260/RX261 Group and the RX210 Group. For details about the functions, refer to section 2, “Comparative Overview of Specifications” and section 5, “Reference Documents”.

Table 1.1 shows a Comparison of Built-In Functions of RX210 Group and RX260/RX261 Group.

Table 1.1 Comparison of Built-In Functions of RX210 Group and RX260/RX261 Group

Function	RX210	RX260/ RX261
CPU	●/▲	
Operating modes	●/■	
Address space	▲/■	
Resets	■	
Option-setting memory (OFSM)	●/▲/■	
Voltage detection circuit (LVDAa): RX210, (LVDAb): RX261	●/▲/■	
Clock generation circuit	●/▲/■	
Clock frequency accuracy measurement circuit (CAC)	●/▲/■	
Low power consumption	●/▲/■	
Register write protection function	●/▲/■	
Exception handling	●/▲	
Interrupt controller (ICUb)	●/▲/■	
Buses	●/▲/■	
Memory protection unit (MPU)	×	○
DMA controller (DMACA)	○	
Data transfer controller (DTCa): RX210, (DTCb): RX261	●	
Event link controller (ELC)	●/▲/■	
I/O ports	●/▲/■	
Multi-function pin controller (MPC)	●/▲/■	
General-purpose PWM timer (GPTWa)	×	○
Port output enable for GPTW (POEGc)	×	○
Multi-function timer pulse unit 2 (MTU2a)	○	×
Port output enable 2 (POE2a)	○	×
16-bit timer pulse unit (TPUa)	○	×
8-bit timer (TMR): RX210, (TMRa): RX261	●	
Compare match timer (CMT)	○	
Realtime clock (RTCb): RX210, (RTCBa): RX261	●/▲/■	
Low power timer (LPTa)	×	○
Watchdog timer (WDTA)	●/■	
Independent watchdog timer (IWDTa)	●/▲/■	
USB 2.0 FS host/function module (USBe)	×	○
Serial communications interface (SCIc, SCId): RX210, (SCIk, SCIh): RX261	●/▲/■	
Serial communications interface (RSCI)	×	○

Function	RX210	RX260/ RX261
I²C bus interface (RIIC): RX210, (RIICa): RX261	▲/■	
CAN FD module (CANFD)	×	○
Serial peripheral interface (RSPI): RX210, (RSPIc): RX261	●/▲/■	
CRC calculator (CRC)	○	
Remote control signal receiver (REMCa)	×	○
Renesas Secure IP (RSIP-E11A)*1	×	○
Capacitive touch sensing unit (CTSU2SLa)	×	○
12-bit A/D converter (S12ADb): RX210, (S12ADE): RX261	●/▲/■	
D/A converter (DA): RX210, (DAa): RX261	●/▲/■	
Temperature sensor (TSMPSa): RX210, (TEMPSA): RX261	●/▲/■	
Comparator A (CMPA)	○	×
Comparator B (CMPB): RX210,(CMPBa): RX261	●/▲	
Data operation circuit (DOC)	●	
RAM	●/▲	
Flash memory (FLASH)/ROM (flash memory for code storage)/E2 DataFlash (flash memory for data storage)	●/▲/■	
Packages	●/■	

Note: 1. Not implemented in RX260 Group products.

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications and a comparison of registers.

In the comparative overview, **red text** indicates specifications which are included only in one of the MCU groups, and specifications that differ between the two groups.

In the register comparison, **red text** indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Register specifications that do not differ are not listed.

2.1 CPU

Table 2.1 shows a Comparative Overview of CPUs.

Table 2.1 Comparative Overview of CPUs

Item	RX210	RX261
CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Eight 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 64 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 111 instructions — Standard built-in instructions: 111 Basic instructions: 77 Single-precision floating-point instructions: 11 DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
FPU	—	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions that conform to the IEEE 754 standard

2.2 Operating Modes

Table 2.2 shows a Comparative Overview of Operating Modes and Table 2.3 shows a Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX210	RX261
Selection of operating modes by the mode setting pins	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
		Boot mode (USB interface)
		Boot mode (FINE interface)
	User boot mode	—
Selection of operating modes by register setting	Single-chip mode, user boot mode	—
	On-chip ROM disabled extended mode	—
	On-chip ROM enabled extended mode	—

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX210	RX261
MDSR	—	Mode status register	—
SYSCR0	—	System control register 0	—

2.3 Address Space

Figure 2.1 shows a Comparative Memory Map of Single-Chip Mode.

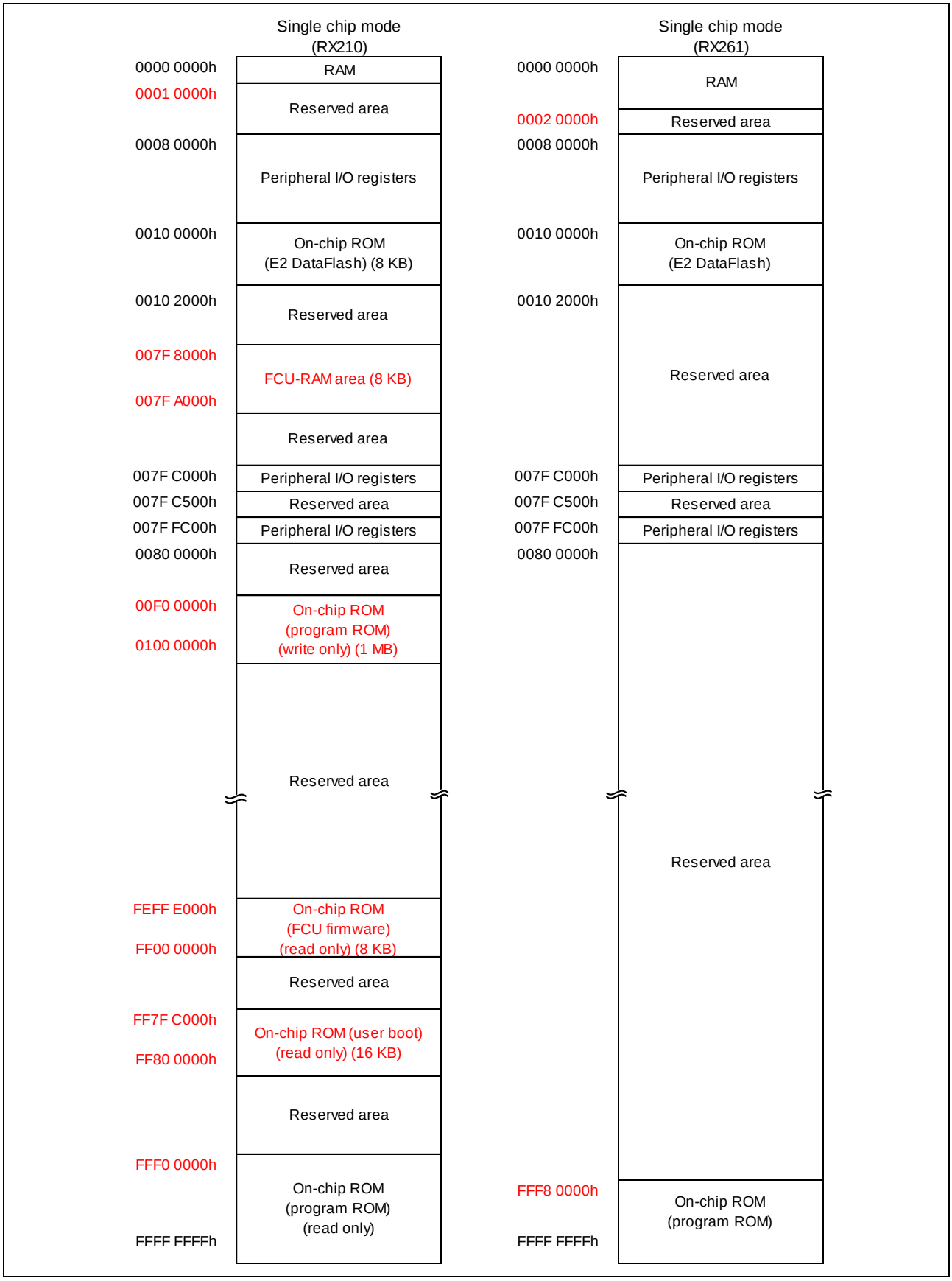

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.4 Resets

Table 2.4 shows a Comparative Overview of Reset Sources and Table 2.5 shows a Comparison of Reset-Related Registers.

Table 2.4 Comparative Overview of Reset Sources

Item	RX210	RX261
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage monitored: VPOR)
Voltage monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage monitored: Vdet0)
Voltage monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage monitored: Vdet1)
Voltage monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage monitored: Vdet2)
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	—
Independent watchdog timer reset	The independent watchdog timer underflows or a refresh error occurs.	The independent watchdog timer underflows or a refresh error occurs.
Watchdog timer reset	The watchdog timer underflows or a refresh error occurs.	The watchdog timer underflows or a refresh error occurs.
Software reset	Register setting	Register setting

Table 2.5 Comparison of Reset-Related Registers

Register	Bit	RX210	RX261
RSTSR0	DPSRSTF	Deep software standby reset detect flag	—

2.5 Option-Setting Memory

Figure 2.2 shows a Comparison of Option-Setting Memory Areas and Table 2.6 shows a Comparison of Option-Setting Memory Registers.

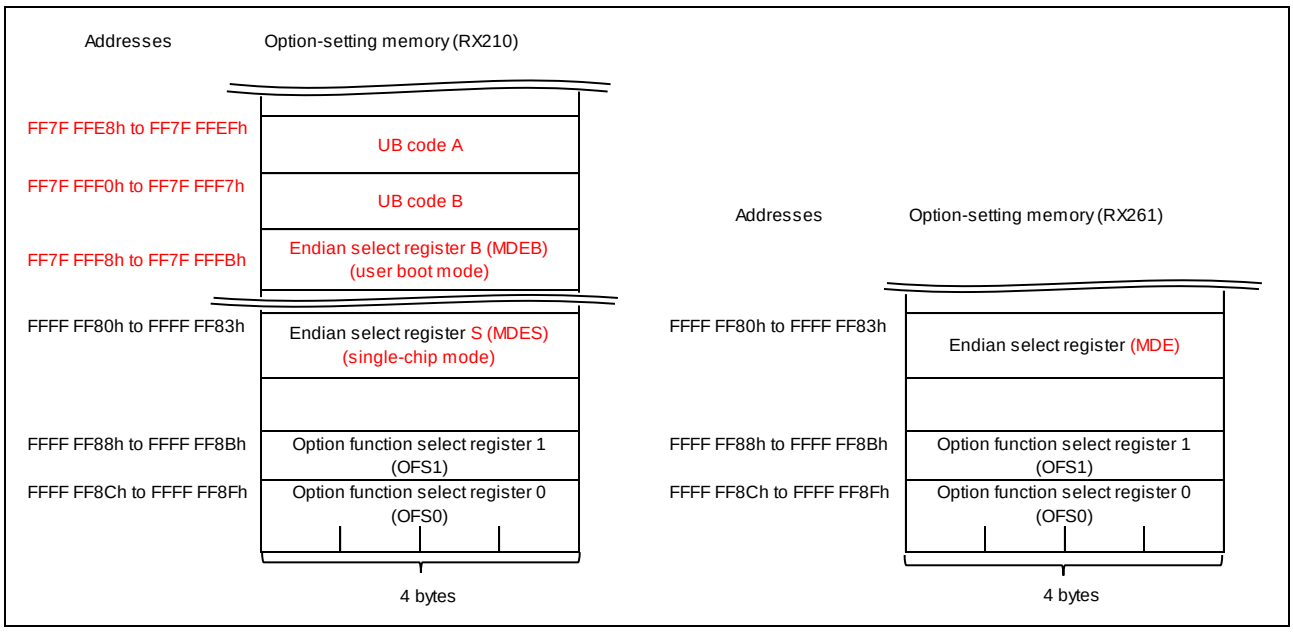

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.6 Comparison of Option-Setting Memory Registers

Register	Bit	RX210 (OFSM)	RX261 (OFSM)
OFS0	WDTTOPS[1:0]	WDT timeout period select bits b3 b2 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	WDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep mode, software standby mode, or deep sleep mode
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.80 V is selected 0 1: 2.80 V is selected 1 0: 1.90 V is selected 1 1: 1.72 V is selected	Voltage detection 0 level select bits b1 b0 0 0: 3.85 V is selected 0 1: 2.85 V is selected 1 0: 2.53 V is selected 1 1: 1.90 V is selected
	FASTSTUP	—	Power-on fast startup time bit
	VDSEL2	—	Voltage detection 0 level select bit 2
	HOCOFRQ[1:0]	—	HOCO frequency select bits

Register	Bit	RX210 (OFSM)	RX261 (OFSM)
MDE	—	—	Endian select register
MDEB	—	Endian select register B	—
MDES	—	Endian select register S	—

2.6 Voltage Detection Circuit

Table 2.7 shows a Comparative Overview of Voltage Detection Circuits and Table 2.8 shows a Comparison of Voltage Detection Circuit Registers.

Table 2.7 Comparative Overview of Voltage Detection Circuits

Item		RX210 (LVDa)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2
				Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.			Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.
	Detection voltage	Selectable from four levels using the OFS1 register	Selectable from sixteen levels using LVDLVLR.LVD1LVL[3:0] bits	Varies according to whether VCC or the CMPA2 pin is selected for voltage input. Selectable from 16 levels using LVDLVLR.LVD2LVL[3:0] bits	Selectable from five levels using the OFS1 register	Selectable from 16 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits

Item		RX210 (LVDa)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitoring flags	—	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection		LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2 pin: CPU restart timing selectable among after specified time with VCC or CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or CMPA2 pin

Item		RX210 (LVDa)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Interrupts	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC or CMPA2 pin, VCC or CMPA2 pin > Vdet2, or both
Digital filter	Enable/ Disable switching	Digital filter function not available	Available	Available	—	—	—
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—	—	—
Event link function		—	Available Event output at Vdet1 passage detection	Available Event output at Vdet2 passage detection	—	Available Event output at Vdet1 passage detection	Available Event output at Vdet2 passage detection

Table 2.8 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX210 (LVDAa)	RX261 (LVDAb)
LVD1CR1	—	Voltage monitoring 1 circuit/comparator A1 control register 1	Voltage monitoring 1 circuit control register 1
LVD1SR	—	Voltage monitoring 1 circuit/comparator A1 status register	Voltage monitoring 1 circuit status register
LVD2CR1	—	Voltage monitoring 2 circuit/comparator A2 control register 1	Voltage monitoring 2 circuit control register 1
LVD2SR	—	Voltage monitoring 2 circuit/comparator A2 status register	Voltage monitoring 2 circuit status register
LVCMPCR	—	Voltage monitoring circuit/comparator A control register	Voltage monitoring circuit control register
	EXVREFINP1	Comparator A1 reference voltage external input select bit	—
	EXVCCINP1	Comparator A1 comparison voltage external input select bit	—
	EXVREFINP2	Comparator A2 reference voltage external input select bit	—
	LVD1E	Voltage detection 1/comparator A1 enable bit 0: Voltage detection 1/comparator A1 circuit disabled 1: Voltage detection 1/comparator A1 circuit enabled	Voltage detection 1 enable bit 0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled
	LVD2E	Voltage detection 2/comparator A2 enable bit 0: Voltage detection 2/comparator A2 circuit disabled 1: Voltage detection 2/comparator A2 circuit is enabled	Voltage detection 2 enable bit 0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled

Register	Bit	RX210 (LVDAa)	RX261 (LVDAb)
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during voltage drop) b3 b0 0 0 0 0: 4.15 V 0 0 0 1: 4.00 V 0 0 1 0: 3.85 V 0 0 1 1: 3.70 V 0 1 0 0: 3.55 V 0 1 0 1: 3.40 V 0 1 1 0: 3.25 V 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V	Voltage detection 1 level select bits (Standard voltage during voltage drop) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.16 V 0 0 1 0: 4.03 V 0 0 1 1: 3.86 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.80 V 1 0 0 0: 2.68 V 1 0 0 1: 2.59 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V 1 1 1 0: 1.75 V 1 1 1 1: 1.65 V Settings other than the preceding are prohibited.
LVDLVLR	LVD2LVL[3:0] (RX210) LVD2LVL[1:0] (RX261)	Voltage detection 2 level select bits (Standard voltage during voltage drop) (b4 to b7) (When LVCMPCR.EXVCCINP2 = 0 (VCC select)) b7 b4 0 0 0 0: 4.15 V 0 0 0 1: 4.00 V 0 0 1 0: 3.85 V 0 0 1 1: 3.70 V 0 1 0 0: 3.55 V 0 1 0 1: 3.40 V 0 1 1 0: 3.25 V 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V (When LVCMPCR.EXVCCINP2 = 1 (CMPA2 pin select)) b7 b4 0 0 0 1: 1.33 V Settings other than the preceding are prohibited.	Voltage detection 2 level select bits (Standard voltage during voltage drop) (b4 and b5) b5 b4 0 0: 4.32 V 0 1: 4.17 V 1 0: 4.03 V 1 1: 3.84 V

Register	Bit	RX210 (LVDAa)	RX261 (LVDAb)
LVD1CR0	—	Voltage monitoring 1 circuit/comparator A1 control register 0	Voltage monitoring 1 circuit control register 0
LVD2CR0	—	Voltage monitoring 2 circuit/comparator A2 control register 0	Voltage monitoring 2 circuit control register 0

2.7 Clock Generation Circuit

Table 2.9 shows a Comparative Overview of Clock Generation Circuits and Table 2.10 shows a Comparison of Clock Generation Circuit Registers.

Table 2.9 Comparative Overview of Clock Generation Circuits

Item	RX210	RX261
Uses	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKB and PCLKD) supplied to peripheral modules. PCLKD is the operating clock for the S12AD module, and PCLKB is the operating clock for modules other than S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the dedicated RTC sub-clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) supplied to the CANFD (message buffer RAM) and GPTW. • Generates the peripheral module clock (PCLKB) supplied to peripheral modules. • Generates the peripheral module (for analog conversion) clock (PCLKD) supplied to the S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the CANFD clock (CANFDCLK) supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) supplied to the CANFD. • Generates the LPT clock (LPTCLK) supplied to the LPT. • Generates the REMC clock (REMCLK) supplied to the REMC.
Operating frequencies	• ICLK: 50 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 50 MHz (max.) • FCLK: — 4 MHz to 32 MHz (when programming and erasing ROM and E2 DataFlash) — 32 MHz (max.) (when reading from E2 DataFlash) • BCLK: 25 MHz (max.) • BCLK pin output: 12.5 MHz (max.)	• ICLK: 64 MHz (max.) • PCLKA: 64 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 64 MHz (max.) • FCLK: — 1 MHz to 64 MHz (when programming and erasing ROM and E2 DataFlash) — 64 MHz (max.) (when reading from E2 DataFlash) • UCLK: 48 MHz • CANFDCLK: 32 MHz (max.) • CANFDMCLK: 20 MHz (max.)

Item	RX210	RX261
Operating frequencies	• CACCLK: Same frequency as each oscillator. • RTCSCLK: 32.768 kHz • IWDTCLK: 125 kHz	• LPTCLK: — 32.768 kHz (when sub-clock is selected) — 15 kHz (when the IWDT-dedicated clock (IWDTCLK) is selected) — 1 MHz (when the LOCO clock (divided by 4) is selected) • REMCLK: The same frequency as that of the selected oscillator. • CACCLK: The same frequency as that of the selected oscillator. • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU output can be forcibly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and the GPTW pin can be forcibly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal resonator • Connection pins: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • External clock input frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal resonator • Connection pins: XCIN, XCOUT • Sub-clock external input pin: EXCIN • Drive capacity switching function
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable between 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, and 24 • VCO oscillation frequency: 50 MHz to 100 MHz	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable between 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (in increments of 0.5) • Oscillation frequency: 24 MHz to 64 MHz

Item	RX210	RX261
PLL2 circuit	—	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable between 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (in increments of 0.5) • Oscillation frequency: 24 MHz to 64 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 32 MHz/36.864 MHz/40 MHz/50 MHz • HOCO power supply control	• Oscillation frequency: 24 MHz, 32 MHz, 48 MHz, 64 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 15 kHz
Control of output on the BCLK pin	• BCLK clock output or high-level output can be selected. • BCLK or BCLK/2 can be selected for output clock.	—

Table 2.10 Comparison of Clock Generation Circuit Registers

Register	Bit	RX210	RX261
SCKCR	—	Reserved (b7 to b4) These bits should be set to 0001.	Reserved (b7 to b4) These bits are read as 0. The write value must be 0.
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
	BCK[3:0]	External bus clock (BCLK) select bits	—
	PSTOP1	BCLK pin output control bit	—
SCKCR3	CKSEL[2:0]	Clock source select bits [Chip version A] b10 b8 0 0 0: LOCO is selected 0 0 1: HOCO is selected 0 1 1: Sub-clock oscillator is selected 1 0 0: PLL circuit is selected [Chip versions B and C] b10 b8 0 0 0: LOCO is selected 0 0 1: HOCO is selected 0 1 0: Main clock oscillator is selected 0 1 1: Sub-clock oscillator is selected 1 0 0: PLL circuit is selected Settings other than the preceding are prohibited.	Clock source select bits b10 b8 0 0 0: LOCO is selected 0 0 1: HOCO is selected 0 1 0: Main clock oscillator is selected 0 1 1: Sub-clock oscillator is selected 1 0 0: PLL circuit is selected Settings other than the preceding are prohibited.

Register	Bit	RX210	RX261
VRCR	—	Voltage regulator control register	—
PLLCR	STC[4:0] (RX210) STC[5:0] (RX261)	Frequency multiplication factor select bits b12 b8 0 0 1 1 1: ×8 0 1 0 0 1: ×10 0 1 0 1 1: ×12 0 1 1 1 1: ×16	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5
PLLCR	STC[4:0] (RX210) STC[5:0] (RX261)	b12 b8 1 0 0 1 1: ×20 1 0 1 1 1: ×24 1 1 0 0 0: ×25 Settings other than the preceding are prohibited.	b13 b8 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 Settings other than the preceding are prohibited.
BCKCR	—	External bus clock control register	—
PLL2CR	—	—	PLL2 control register
PLL2CR2	—	—	PLL2 control register 2
SOSCCR	SOSTP	Sub-clock oscillator stop bit	Sub-clock oscillator stop bit
		The initial value after a reset differs.	
OSCOVFSR	—	—	Oscillation stabilization flag register
CKOCR	—	—	CLKOUT output control register
HOCOCR2	—	High-speed on-chip oscillator control register 2	—

Register	Bit	RX210	RX261
OSTDCR	OSTDIE	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled. Oscillation stop detection is not notified to the POE. 1: The oscillation stop detection interrupt is enabled. Oscillation stop detection is notified to the POE.	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled. Oscillation stop detection is not notified to the POEG. 1: The oscillation stop detection interrupt is enabled. Oscillation stop detection is notified to the POEG.
LOFCR	—	—	Low-speed on-chip oscillator forced oscillation control register
LOCOTRR2	—	—	Low-speed on-chip oscillator trimming register 2
ILOCOTRR	—	—	IWDT-dedicated on-chip oscillator trimming register
HOCOTRR0	—	—	High-speed on-chip oscillator trimming register 0
CANFDCKDIVCR	—	—	CANFD clock division control register
USBCKCR	—	—	USB clock control register
CANFDCKCR	—	—	CANFD clock control register
SOMCR	—	—	Sub-clock oscillator mode control register
MOSCWTCR	—	—	Main clock oscillator wait control register
MOFCR	MODRV[2:0]	Main clock oscillator drive capability switch bits	—
	MODRV21	—	Main clock oscillator drive capability switch bit
	MODRV2[1:0]	Main clock oscillator drive capability switch 2 bits	—
HOCOPCR	—	High-speed on-chip oscillator power supply control register	—
PLLPCR	—	PLL power control register	—

2.8 Clock Frequency Accuracy Measurement Circuit

Table 2.11 shows a Comparative Overview of Clock Frequency Accuracy Measurement Circuits and Table 2.12 shows a Comparison of Clock Frequency Accuracy Measurement Circuit Registers.

Table 2.11 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX210 (CAC)	RX261 (CAC)
Measurement target clocks	The frequency of the following clocks can be measured: • Output clock of main clock oscillator (main clock) • Output clock of sub-clock oscillator (sub-clock) • Output clock of high-speed on-chip oscillator (HOCO clock) • Output clock of low-speed on-chip oscillator (LOCO clock) • Output clock of IWDT-dedicated on-chip oscillator (IWDTCLK clock)	The frequency of the following clocks can be measured: • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Measurement reference clocks	—	• External clock input to the CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Selectable functions	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to enable module stop state	Ability to enable module stop state

Table 2.12 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX210 (CAC)	RX261 (CAC)
CACR1	FMCS[2:0]	Frequency measurement clock select bits [Chip version A] b3 b1 0 0 1: Output clock of sub-clock oscillator 0 1 0: Output clock of high-speed on-chip oscillator 0 1 1: Output clock of low-speed on-chip oscillator 1 0 0: Output clock of IWDT-dedicated on-chip oscillator [Chip versions B and C] b3 b1 0 0 0: Output clock of main clock oscillator 0 0 1: Output clock of sub-clock oscillator 0 1 0: Output clock of high-speed on-chip oscillator 0 1 1: Output clock of low-speed on-chip oscillator 1 0 0: Output clock of IWDT-dedicated on-chip oscillator Settings other than the preceding are prohibited.	Frequency measurement clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the preceding are prohibited.
CACR2	RSCS[2:0]	Reference signal generation clock select bits [Chip version A] b3 b1 0 0 1: Output clock of sub-clock oscillator 0 1 0: Output clock of high-speed on-chip oscillator 0 1 1: Output clock of low-speed on-chip oscillator 1 0 0: Output clock of IWDT-dedicated on-chip oscillator	Measurement reference clock select bits

Register	Bit	RX210 (CAC)	RX261 (CAC)
CACR2	RSCS[2:0]	[Chip versions B and C] b3 b1 0 0 0: Output clock of main clock oscillator 0 0 1: Output clock of sub-clock oscillator 0 1 0: Output clock of high-speed on-chip oscillator 0 1 1: Output clock of low-speed on-chip oscillator 1 0 0: Output clock of IWDT-dedicated on-chip oscillator Settings other than the preceding are prohibited.	 b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the preceding are prohibited.

2.9 Low Power Consumption

Table 2.13 shows a Comparative Overview of Low Power Consumption Functions, Table 2.14 shows a Comparison of Methods for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.15 shows a Comparison of Low Power Consumption Registers.

Table 2.13 Comparative Overview of Low Power Consumption Functions

Item	RX210	RX261
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKD), and FlashIF clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	—
Module stop function	Functions can be stopped independently for each peripheral module.	Functions can be stopped independently for each peripheral module.
Function for transition to low power consumption mode	The CPU, peripheral modules, or oscillators can be stopped to enter a low power consumption state.	The CPU, peripheral modules, or oscillators can be stopped to enter a low power consumption state.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • Deep sleep mode • Software standby mode • Snooze mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. [Chip versions A and C] • Five operating power control modes are available: — High-speed operating mode — Middle-speed operating mode 1A — Middle-speed operating mode 1B — Low-speed operating mode 1 — Low-speed operating mode 2 [Chip version B] • Seven operating power control modes are available: — High-speed operating mode — Middle-speed operating mode 1A — Middle-speed operating mode 1B — Middle-speed operating mode 2A — Middle-speed operating mode 2B — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, deep sleep mode, and snooze mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Four operating power control modes are available: — High-speed operating mode — Middle-speed operating mode — Middle-speed operating mode 2 — Low-speed operating mode

Table 2.14 Comparison of Methods for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX261
Sleep mode	Enter method	Control register + instruction	Control register + instruction
	Exit method other than reset	Interrupt	Interrupt
	State after exit	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operating possible	Operating possible
	Sub-clock oscillator	Operating possible	Operating possible
	High-speed on-chip oscillator	Operating possible	Operating possible
	Low-speed on-chip oscillator	Operating possible	Operating possible
	IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
	PLL	Operating possible	Operating possible
	PLL2	—	Operating possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh): RX210 (0000 0000h to 0001 FFFFh): RX261 RAM1 (0001 0000h to 0001 FFFFh): RX210	Operating possible (retained)	Operating possible (retained)
	DMAC	—	Operating possible
	DTC	—	Operating possible
	Flash memory	Operating	Operating
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operating possible	Operating possible
	Remote control signal receiver (REMC)	—	Operating possible
	Realtime clock (RTC)	Operating possible	Operating possible
	Low power timer (LPT)	—	Operating possible
	8-bit timer (unit 0, unit 1) (TMR)	Operating possible	—
	Voltage detection circuit (LVD)	Operating possible	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Operating possible	Operating possible
	I/O ports	Operating	Operating
	RTCOUT output	—	Operating possible
	CLKOUT output	—	Operating possible
	Comparator B	—	Operating possible
All-module clock stop mode	Enter method	Control register + instruction	—
	Exit method other than reset	Interrupt	—
	State after exit	Program execution state (interrupt processing)	—
	Main clock oscillator	Operating possible	—
	Sub-clock oscillator	Operating possible	—
	High-speed on-chip oscillator	Operating possible	—
	Low-speed on-chip oscillator	Operating possible	—
	IWDT-dedicated on-chip oscillator	Operating possible	—
	PLL	Operating possible	—
	CPU	Stopped (retained)	—

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX261
All-module clock stop mode	RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh)	Stopped (retained)	—
	Flash memory	Stopped (retained)	—
	Watchdog timer (WDT)	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operating possible	—
	Realtime clock (RTC)	Operating possible	—
	8-bit timer (unit 0, unit 1) (TMR)	Operating possible	—
	Voltage detection circuit (LVD)	Operating possible	—
	Power-on reset circuit	Operating	—
	Peripheral modules	Stopped (retained)	—
	I/O ports	Retained	—
Deep sleep mode	Enter method	—	Control register + instruction
	Exit method other than reset	—	Interrupt
	State after exit	—	Program execution state (interrupt processing)
	Main clock oscillator	—	Operating possible
	Sub-clock oscillator	—	Operating possible
	High-speed on-chip oscillator	—	Operating possible
	Low-speed on-chip oscillator	—	Operating possible
	IWDT-dedicated on-chip oscillator	—	Operating possible
	PLL	—	Operating possible
	PLL2	—	Operating possible
	CPU	—	Stopped (retained)
	RAM0 (0000 0000h to 0001 FFFFh)	—	Stopped (retained)
	DMAC	—	Stopped (retained)
	DTC	—	Stopped (retained)
	Flash memory	—	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operating possible
	Remote control signal receiver (REMC)	—	Operating possible
	Realtime clock (RTC)	—	Operating possible
	Low power timer (LPT)	—	Operating possible
	Voltage detection circuit (LVD)	—	Operating possible
	Power-on reset circuit	—	Operating
	Peripheral modules	—	Operating possible
	I/O ports	—	Operating
	RTCOUT output	—	Operating possible
	CLKOUT output	—	Operating possible
	Comparator B	—	Operating possible
Software standby mode	Enter method	Control register + instruction	Control register + instruction
	Exit method other than reset	Interrupt	Interrupt
	State after exit	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX261
Software standby mode	Sub-clock oscillator	Operating possible	Operating possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Operating possible
	IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
	PLL	Stopped	Stopped
	PLL2	—	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh): RX210 (0000 0000h to 0001 FFFFh): RX261 RAM1 (0001 0000h to 0001 7FFFh): RX210	Stopped (retained)	Stopped (retained)
	DMAC	—	Stopped (retained)
	DTC	—	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operating possible	Operating possible
	Remote control signal receiver (REMC)	—	Operating possible
	Realtime clock (RTC)	Operating possible	Operating possible
	Low power timer (LPT)	—	Operating possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	—
	Voltage detection circuit (LVD)	Operating possible	Operating possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	RTCOUT output	—	Operating possible
	CLKOUT output	—	Operating possible
	Comparator B	—	Operating possible
Deep software standby mode	Enter method	Control register + instruction	—
	Exit method other than reset	Interrupt	—
	State after exit	Program execution state (reset processing)	—
	Main clock oscillator	Stopped	—
	Sub-clock oscillator	Operating possible	—
	High-speed on-chip oscillator	Stopped	—
	Low-speed on-chip oscillator	Stopped	—
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	—
	PLL	Stopped	—
	CPU	Stopped (undefined)	—
	RAM0 (0000 0000h to 0000 FFFFh) RAM1 (0001 0000h to 0001 7FFFh)	Stopped (undefined)	—
	Flash memory	Stopped (retained)	—
	Watchdog timer (WDT)	Stopped (undefined)	—

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX210	RX261
Deep software standby mode	Independent watchdog timer (IWDT)	Stopped (undefined)	—
	Realtime clock (RTC)	Operating possible	—
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (undefined)	—
	Voltage detection circuit (LVD)	Operating possible	—
	Power-on reset circuit	Operating	—
	Peripheral modules	Stopped (undefined)	—
	I/O ports	Retained	—
Snooze mode	Enter method	—	The condition that enters snooze mode is met while in software standby mode
	Exit method other than reset	—	Interrupt or condition that exits snooze mode is met
	State after exit	—	Program execution state (interrupt processing) or software standby mode
	Main clock oscillator	—	Operating possible
	Sub-clock oscillator	—	Operating possible
	High-speed on-chip oscillator	—	Operating possible
	Low-speed on-chip oscillator	—	Operating possible
	IWDT-dedicated on-chip oscillator	—	Operating possible
	PLL	—	Operating possible
	PLL2	—	Operating possible
	CPU	—	Stopped (retained)
	RAM0 (0000 0000h to 0000 FFFFh): RX210 (0000 0000h to 0001 FFFFh): RX261	—	Operating possible (retained)
	DMAC	—	Stopped (retained)
	DTC	—	Operating possible
	Flash memory	—	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operating possible
	Realtime clock (RTC)	—	Operating possible
	Low power timer (LPT)	—	Operating possible
	Remote control signal receiver (REMC)	—	Operating possible
	Voltage detection circuit (LVD)	—	Operating possible
	Power-on reset circuit	—	Operating
	Peripheral modules	—	Operating possible
	I/O ports	—	Operating
	RTCOUT output	—	Operating possible
	CLKOUT output	—	Operating possible
	Comparator B	—	Operating possible

Note: “Operating possible” indicates that the control register setting determines whether the state is operating or stopped.
“Stopped (retained)” indicates that internal operations are suspended with internal register values retained.

Table 2.15 Comparison of Low Power Consumption Registers

Register	Bit	RX210	RX261
SBYCR	OPE	Output port enable bit	—
	SSBY	Software standby bit 0: Enters sleep mode or all-module clock stop mode after the WAIT instruction is executed. 1: Enters software standby mode after the WAIT instruction is executed.	Software standby bit 0: Enters sleep mode or deep sleep mode after the WAIT instruction is executed. 1: Enters software standby mode after the WAIT instruction is executed.
MSTPCRA	MSTPA7	—	General-purpose PWM timer module stop bit
	MSTPA9	Multi-function timer pulse unit module stop bit	—
	MSTPA13	16-bit timer pulse unit module stop bit	—
	MSTPA24	Module stop A24 bit	—
	MSTPA27	Module stop A27 bit	—
	MSTPA29	Module stop A29 bit	—
	ACSE	All-module clock stop mode enable bit	—
MSTPCRB	MSTPB8	Temperature sensor module stop bit	—
	MSTPB19	—	USB 2.0 FS host/function module stop bit
	MSTPB24	Serial communication interface 7 module stop bit	—
	MSTPB27	Serial communication interface 4 module stop bit	—
	MSTPB28	Serial communication interface 3 module stop bit	—
	MSTPB29	Serial communication interface 2 module stop bit	—
MSTPCRC	MSTPC0	RAM0 module stop bit Target module: RAM0 (0000 0000h to 0000 FFFFh)	RAM0 module stop bit Target module: RAM0 (0000 0000h to 0001 FFFFh)
	MSTPC1	RAM1 module stop bit	—
	MSTPC24	Serial communication interface 11 module stop bit	—
	MSTPC25	Serial communication interface 10 module stop bit	—
	MSTPC29	—	Remote control signal receiver module stop bit
	DSLPE	—	Deep sleep mode enable bit
MSTPCRD	—	—	Module stop control register D

Register	Bit	RX210	RX261
OPCCR	OPCM[2:0]	Operating power control mode select bits [Chip versions A and C] b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1A 0 1 1: Middle-speed operating mode 1B 1 1 0: Low-speed operating mode 1 1 1 1: Low-speed operating mode 2 [Chip version B] b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1A 0 1 1: Middle-speed operating mode 1B 1 0 0: Middle-speed operating mode 2A 1 0 1: Middle-speed operating mode 2B 1 1 0: Low-speed operating mode 1 1 1 1: Low-speed operating mode 2 Settings other than the preceding are prohibited.	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1 0 0: Middle-speed operating mode 2 Settings other than the preceding are prohibited.
	OPCMTSF	Operating power control mode transition status flag • Read 0: Transition completed 1: During transition • Write The write value must be 0.	Operating power control mode transition status flag 0: Transition completed 1: During transition
SOPCCR	—	—	Sub operating power control register
RSTCKCR	RSTCKSEL [2:0]	Sleep mode return clock source select bits [Chip version A] b2 b0 0 0 1: HOCO is selected [Chip versions B and C] b2 b0 0 0 1: HOCO is selected 0 1 0: Main clock oscillator is selected When the RSTCKEN bit is set to 1, settings other than the preceding are prohibited.	Sleep mode return clock source select bits b2 b0 0 0 0: LOCO is selected 0 0 1: HOCO is selected 0 1 0: Main clock oscillator is selected When the RSTCKEN bit is set to 1, settings other than the preceding are prohibited.
SNZCR	—	—	Snooze control register
SNZCR2	—	—	Snooze control register 2

Register	Bit	RX210	RX261
RPSCR	—	—	RAM power-saving control register
MOSCWTCR	—	Main clock oscillator wait control register	—
SOSCWTCR	—	Sub-clock oscillator wait control register	—
PLLWTCR	—	PLL wait control register	—
HOCOWTCR2	—	HOCO wait control register 2	—
DPSBYCR	—	Deep standby control register	—
DPSIER0	—	Deep standby interrupt enable register 0	—
DPSIER2	—	Deep standby interrupt enable register 2	—
DPSIFR0	—	Deep standby interrupt flag register 0	—
DPSIFR2	—	Deep standby interrupt flag register 2	—
DPSIEGR0	—	Deep standby interrupt edge register 0	—
DPSIEGR2	—	Deep standby interrupt edge register 2	—
FHSSBYCR	—	Flash HOCO software standby control register	—
DPSBKRy (y = 0 to 31)	—	Deep standby backup register	—

2.10 Register Write Protection Functions

Table 2.16 shows a Comparative Overview of Register Write Protection Functions and Table 2.17 shows a Comparison of Register Write Protection Registers.

Table 2.16 Comparative Overview of Register Write Protection Functions

Item	RX210	RX261
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, PLL2CR, PLL2CR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, LOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR2, ILOCOTRR, HOCOTRR0, SOMCR, CANFDCKCR, CANFDCKDIVCR, USBCKCR
PRC1 bit	• Register related to operating modes: SYSCR0, SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, MOSCWTCR, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, HOCOWTCR2 • Registers related to the clock generation circuit: MOFCR, HOCOPCR, PLLPCR (for chip version B) • Software reset register: SWRR	• Register related to operating modes: SYSCR1 • Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR, RPSCR, SNZCR, SNZCR2 • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	• VRCR register	• Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPCMR1, LPWUCR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.17 Comparison of Register Write Protection Registers

Register	Bit	RX210	RX261
PRCR	PRC1	Protect bit 1 Enables writing to the registers related to operating modes, low power consumption, and software reset. 0: Write disabled 1: Write enabled	Protect bit 1 Enables writing to the registers related to operating modes, low power consumption, clock generation circuit, and software reset. 0: Write disabled 1: Write enabled
	PRC2	Protect bit 2 Enables writing to the VRCR register. 0: Write disabled 1: Write enabled	Protect bit 2 Enables writing to the registers related to the low power timer. 0: Write disabled 1: Write enabled

2.11 Exception Handling

Table 2.18 shows a Comparative Overview of Exception Handling, Table 2.19 shows a Comparison of Vectors, and Table 2.20 shows a Comparison of Instructions for Returning from Exception Handling Routines.

Table 2.18 Comparative Overview of Exception Handling

Item	RX210	RX261
Exception events	• Undefined instruction exception • Privileged instruction exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Single-precision floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.19 Comparison of Vectors

Item		RX210	RX261
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		—	Exception vector table (EXTB)
Single-precision floating-point exception		—	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.20 Comparison of Instructions for Returning from Exception Handling Routines

Item		RX210	RX261
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		—	RTE
Floating-point exception		—	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.12 Interrupt Controllers

Table 2.21 shows a Comparative Overview of Interrupt Controllers and Table 2.22 shows a Comparison of Interrupt Controller Registers.

Table 2.21 Comparative Overview of Interrupt Controllers

Item		RX210 (ICUb)	RX261 (ICUb)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each connected peripheral module source.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each connected peripheral module source.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level, falling edge, rising edge, or rising and falling edges can be set at the source level. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level, falling edge, rising edge, or rising and falling edges can be set at the source level. • Digital filter function: Supported
	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• Interrupt generated by writing to a register • Number of sources: 1
	Event link interrupts	An ELSR18I or ELSR19I interrupt can be generated by an ELC event.	An ELSR8I, ELSR18I, or ELSR19I interrupt can be generated by an ELC event.
	Interrupt priority	Priority is set by register.	Priority is set by register.
	Fast interrupt function	Faster CPU interrupt handling can be enabled. This can be enabled for a single interrupt source only.	Faster CPU interrupt handling can be enabled. This can be enabled for a single interrupt source only.
	DTC and DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupt	NMI pin interrupt	• Interrupts from NMI pins • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Supported	• Interrupts from NMI pins • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	An interrupt is generated when an oscillation stop is detected.	An interrupt is generated when an oscillation stop is detected.
	WDT underflow/ refresh error interrupt	An interrupt is generated by underflow of the down counter or a refresh error.	An interrupt is generated by underflow of the down counter or a refresh error.
	IWDT underflow/ refresh error interrupt	An interrupt is generated by underflow of the down counter or a refresh error.	An interrupt is generated by underflow of the down counter or a refresh error.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)

Item		RX210 (ICUb)	RX261 (ICUb)
Non-maskable interrupt	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)
	RAM error interrupt	—	An interrupt is generated when a RAM parity check error is detected.
Return from low power consumption modes	Sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Return is initiated by any non-maskable interrupt and any other interrupt.
	Deep sleep mode	—	Return is initiated by any non-maskable interrupt and any other interrupt.
	All-module clock stop mode	Return is initiated by a non-maskable interrupt, IRQ0 to IRQ7 interrupt, TMR interrupt, or an RTC alarm or periodic interrupt.	—
	Software standby mode	Return is initiated by a non-maskable interrupt, IRQ0 to IRQ7 interrupt, or an RTC alarm or periodic interrupt.	Return is initiated by an NMI pin interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral function interrupt (IWDT, voltage monitoring 1, voltage monitoring 2, RTC alarm or periodic interrupt, REMC, USB0 resume), or ELSR8I interrupt (LPT dedicated interrupt).
	Snooze mode	—	Return is initiated by an NMI pin interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral function interrupt (IWDT, voltage monitoring 1, voltage monitoring 2, RTC alarm or periodic interrupt, REMC, USB0 resume), or SNZI interrupt (snooze release interrupt).

Table 2.22 Comparison of Interrupt Controller Registers

Register	Bit	RX210 (ICUb)	RX261 (ICUb)
IPRn	—	Interrupt source priority register n (n = 000 to 250)	Interrupt source priority register n (n = interrupt vector number)
NMISR	RAMST	—	RAM error interrupt status flag
NMIER	RAMEN	—	RAM error interrupt enable bit

2.13 Buses

Table 2.23 shows a Comparative Overview of Buses and Table 2.24 shows a Comparison of Bus-Related Registers.

Table 2.23 Comparative Overview of Buses

Item		RX210	RX261
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	• Connected to RAM	• Connected to RAM
	Memory bus 2	• Connected to ROM	• Connected to ROM
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to DMAC and DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral modules other than internal peripheral bus 1) • Operates in synchronization with the peripheral module clocks (PCLKB and PCLKD)	• Connected to peripheral modules (peripheral modules other than internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 3	—	• Connected to peripheral modules (USB0, CANFD, CTSU, REMC, and RSCI) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	—	• Connected to the peripheral module (GPTW) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	—	• Connected to peripheral modules (CANFD (message buffer RAM)) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external bus clock (BCLK)	—

Table 2.24 Comparison of Bus-Related Registers

Register	Bit	RX210	RX261
CSnCR	—	CSn control register (n = 0 to 3)	—
CSnREC	—	CSn recovery cycle register (n = 0 to 3)	—
CSRECEN	—	CS recovery cycle insertion enable register	—
CSnMOD	—	CSn mode register (n = 0 to 3)	—
CSnWCR1	—	CSn wait control register 1 (n = 0 to 3)	—
CSnWCR2	—	CSn wait control register 2 (n = 0 to 3)	—
BUSPRI	BPGB[1:0]	Internal peripheral bus 2 priority control bits	Internal peripheral buses 2 and 3 priority control bits
	BPHB[1:0]	—	Internal peripheral buses 4 and 5 priority control bits
	BPEB[1:0]	External bus priority control bits	—

2.14 Data Transfer Controller

Table 2.25 shows a Comparative Overview of Data Transfer Controllers and Table 2.26 shows a Comparison of Data Transfer Controller Registers.

Table 2.25 Comparative Overview of Data Transfer Controllers

Item	RX210 (DTCa)	RX261 (DTCb)
Number of transfer channels	—	Equal to the total number of interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size — The maximum repeat size is 256. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 data units.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits, or 1,024 bytes.
Transfer channel	• Channel transfer corresponding to the interrupt source is possible. (transferred by a DTC activation request from the ICU).	—
Chain transfer function	• Data of multiple channels can be transferred in response to a single trigger source. • Either “executed when the counter is 0” or “always executed” can be selected for chain transfer.	• Multiple types of data transfers can be executed consecutively in response to a single transfer request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected and executed based on the transfer data. • Only one sequence transfer trigger source can be selected at a time. • A maximum of 256 sequences can be specified for a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • An entire sequence can be executed for a single request, or the sequence can be suspended and resumed on the next transfer request (this is called sequence division).

Item	RX210 (DTCa)	RX261 (DTCb)
Transfer space	• Short address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh excepting reserved areas) • Full address mode: 4 GB (Areas from 0000 0000h to FFFF FFFFh excepting reserved areas)	• Short address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh excepting reserved areas) • Full address mode: 4 GB (Areas from 0000 0000h to FFFF FFFFh excepting reserved areas)
Data transfer units	• Length of single data: 8, 16, or 32 bits • Number of data for a single block: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of a specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of a specified number of data units.
Event link function	An event link request is generated after a single data transfer (or after one block for block transfers).	An event link request is generated after a single data transfer (or after one block for block transfers).
Read skip	Read skip of transfer information can be specified.	Reading of transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back skip can be performed if the address of the transfer source or destination is fixed.	Write-back can be skipped for transferred data that is not updated if the address of the transfer source or destination is fixed.
Write-back disable	—	Write-back of transfer information can be disabled.
Displacement addition	—	The displacement value can be added to the source address (selected for each transfer information level).
Low power consumption function	Can transition to module stop state	Can transition to module stop state

Table 2.26 Comparison of Data Transfer Controller Registers

Register	Bit	RX210 (DTCa)	RX261 (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCVBR	—	DTC vector base register The lower 12 bits are reserved and read as 0. The write value must be 0. The address can be set in the range of 0000 0000h to 07FF F000h and F800 0000h to FFFF F000h in 4-KB units.	DTC vector base register The lower 10 bits are reserved and the values are fixed to 0. The write value must be 0. The address can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1-KB units.
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.15 Event Link Controller

Table 2.27 shows a Comparative Overview of Event Link Controllers, Table 2.28 shows a Comparison of Event Link Controller Registers, Table 2.29 shows a Correspondence Between ELSRn Registers and Peripheral Modules, and Table 2.30 shows a Correspondence Between Event Signal Names Set in ELSRn.ELS[7:0] and Signal Numbers.

Table 2.27 Comparative Overview of Event Link Controllers

Item	RX210 (ELC)	RX261 (ELC)
Event link function	• 59 types of event signal can be directly linked to modules. • The operation of timer modules at event input can be selected. • Event link operation is supported for ports B and E. — Single port: Event linkage can be set for a specified 1-bit port. — Port group: Event linkage can be set for a group of specified bits within an 8-bit port.	• 116 types of event signal can be directly linked to peripheral modules. • The operation of timer-related peripheral modules when inputting event signals can be selected. • Event link operation is supported for ports B and E. — Single port: Event linkage can be set for a specified single port. — Port group: Event linkage can be set for a group of specified ports (selected from a maximum of eight ports).
Low power consumption function	Can transition to module stop state	Can transition to module stop state

Table 2.28 Comparison of Event Link Controller Registers

Register	Bit	RX210 (ELC)	RX261 (ELC)
ELSRn	—	Event link setting register n (n = 1 to 4, 7, 10, 12, 15, 16, 18 to 29)	Event link setting register n (n = 7, 8, 10, 12, 14 to 16, 18 to 28, 48 to 56)
	ELS[7:0]	Event link select bits b7 b0 00000000: Event link function is disabled. 00000001 to 01101001: Specify the number of the event signal to be linked. Settings other than the preceding are prohibited.	Event link select bits 00h: Disables event signal output to the applicable peripheral module. 1Fh to C6h: Specify the number of the event signal to be linked. Settings other than the preceding are prohibited.
ELOPA	—	Event link option setting register A	—
ELOPB	—	Event link option setting register B	—
ELOPC	LPTMD[1:0]	—	LPT operation select bits

Table 2.29 Correspondence Between ELSRn Registers and Peripheral Modules

Register	RX210 (ELC)	RX261 (ELC)
ELSR1	MTU1	—
ELSR2	MTU2	—
ELSR3	MTU3	—
ELSR4	MTU4	—
ELSR7	CMT1	CMT1
ELSR8	—	ICU (LPT-dedicated interrupt)
ELSR10	TMR0	TMR0
ELSR12	TMR2	TMR2
ELSR14	—	CTSU
ELSR15	12-bit A/D converter	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	Interrupt 1	ICU (interrupt 1)
ELSR19	Interrupt 2	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switches to LOCO	Clock source switches to LOCO
ELSR29	POE	—
ELSR48	—	GPTW event source A (all channels)
ELSR49	—	GPTW event source B (all channels)
ELSR50	—	GPTW event source C (all channels)
ELSR51	—	GPTW event source D (all channels)
ELSR52	—	GPTW event source E (all channels)
ELSR53	—	GPTW event source F (all channels)
ELSR54	—	GPTW event source G (all channels)
ELSR55	—	GPTW event source H (all channels)
ELSR56	—	S12AD (ELCTRG01N)

Table 2.30 Correspondence Between Event Signal Names Set in ELSRn.ELS[7:0] and Signal Numbers

Value of ELS[7:0] Bits	RX210 (ELC)	RX261 (ELC)
08h	MTU1 compare match 1A signal	—
09h	MTU1 compare match 1B signal	—
0Ah	MTU1 overflow signal	—
0Bh	MTU1 underflow signal	—
0Ch	MTU2 compare match 2A signal	—
0Dh	MTU2 compare match 2B signal	—
0Eh	MTU2 overflow signal	—
0Fh	MTU2 underflow signal	—
10h	MTU3 compare match 3A signal	—
11h	MTU3 compare match 3B signal	—
12h	MTU3 compare match 3C signal	—
13h	MTU3 compare match 3D signal	—
14h	MTU3 overflow signal	—
15h	MTU4 compare match 4A signal	—
16h	MTU4 compare match 4B signal	—
17h	MTU4 compare match 4C signal	—
18h	MTU4 compare match 4D signal	—
19h	MTU4 overflow signal	—
1Ah	MTU4 underflow signal	—
1Fh	CMT1 compare match 1 signal	CMT1 compare match 1
22h	TMR0 compare match A0 signal	TMR0 compare match A0
23h	TMR0 compare match B0 signal	TMR0 compare match B0
24h	TMR0 overflow signal	TMR0 overflow
28h	TMR2 compare match A2 signal	TMR2 compare match A2
29h	TMR2 compare match B2 signal	TMR2 compare match B2
2Ah	TMR2 overflow signal	TMR2 overflow
2Eh	RTC periodic signal	RTC periodic event (Select 1/256 seconds, 1/128 seconds, 1/64 seconds, 1/32 seconds, 1/16 seconds, 1/8 seconds, 1/4 seconds, 1/2 seconds, 1 second, or 2 seconds.)
31h	IWDT underflow/refresh error signal	IWDT underflow/refresh error
32h	—	LPT compare match 0
33h	—	LPT compare match 1
34h	—	S12AD comparison conditions are met
35h	—	S12AD comparison conditions are not met
3Ah	SCI5 error (receive error or error signal detection) signal	SCI5 error (receive error or error signal detection)
3Bh	SCI5 receive data full signal	SCI5 receive data full
3Ch	SCI5 transmit data empty signal	SCI5 transmit data empty
3Dh	SCI5 transmit end signal	SCI5 transmit end
4Eh	RIIC0 communication error or event generation signal	RIIC0 communication error or event generation
4Fh	RIIC0 receive data full signal	RIIC0 receive data full
50h	RIIC0 transmit data empty signal	RIIC0 transmit data empty
51h	RIIC0 transmit end signal	RIIC0 transmit end

Value of ELS[7:0] Bits	RX210 (ELC)	RX261 (ELC)
52h	RSPI0 error (mode fault, overrun, or parity error) signal	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h	RSPI0 idle signal	RSPI0 idle
54h	RSPI0 receive data full signal	RSPI0 receive buffer full
55h	RSPI0 receive data empty signal	RSPI0 transmit buffer empty
56h	RSPI0 transmit end signal (except during clock synchronous operation in slave mode)	RSPI0 transmit end
58h	A/D conversion end signal of 12-bit A/D converter	S12AD A/D conversion end
59h	Comparator B0 comparison result change signal	Comparator B0 comparison result change
5Ah	Comparator B0, B1 common comparison result change signal	Comparator B0, B1 common comparison result change
5Bh	LVD1 voltage detection signal	LVD1 voltage detection
5Ch	LVD2 voltage detection signal	LVD2 voltage detection
5Dh	DMAC0 transfer end signal	DMAC0 transfer end
5Eh	DMAC1 transfer end signal	DMAC1 transfer end
5Fh	DMAC2 transfer end signal	DMAC2 transfer end
60h	DMAC3 transfer end signal	DMAC3 transfer end
61h	DTC transfer end signal	DTC transfer end
62h	Oscillation stop detection signal of clock generation circuit	Oscillation stop detection of clock generation circuit
63h	Input edge detection signal of input port group 1	Input edge detection of input port group 1
64h	Input edge detection signal of input port group 2	Input edge detection of input port group 2
65h	Input edge detection signal of single input port 0	Input edge detection of single input port 0
66h	Input edge detection signal of single input port 1	Input edge detection of single input port 1
67h	Input edge detection signal of single input port 2	Input edge detection of single input port 2
68h	Input edge detection signal of single input port 3	Input edge detection of single input port 3
69h	Software event signal	Software event
6Ah	—	DOC data operation condition met
80h	—	GPTW0 compare match A
81h	—	GPTW0 compare match B
82h	—	GPTW0 compare match C
83h	—	GPTW0 compare match D
84h	—	GPTW0 compare match E
85h	—	GPTW0 compare match F
86h	—	GPTW0 overflow
87h	—	GPTW0 underflow
88h	—	GPTW0 A/D conversion start request A
89h	—	GPTW0 A/D conversion start request B
8Ah	—	GPTW1 compare match A
8Bh	—	GPTW1 compare match B
8Ch	—	GPTW1 compare match C
8Dh	—	GPTW1 compare match D

Value of ELS[7:0] Bits	RX210 (ELC)	RX261 (ELC)
8Eh	—	GPTW1 compare match E
8Fh	—	GPTW1 compare match F
90h	—	GPTW1 overflow
91h	—	GPTW1 underflow
92h	—	GPTW1 A/D conversion start request A
93h	—	GPTW1 A/D conversion start request B
94h	—	GPTW2 compare match A
95h	—	GPTW2 compare match B
96h	—	GPTW2 compare match C
97h	—	GPTW2 compare match D
98h	—	GPTW2 compare match E
99h	—	GPTW2 compare match F
9Ah	—	GPTW2 overflow
9Bh	—	GPTW2 underflow
9Ch	—	GPTW2 A/D conversion start request A
9Dh	—	GPTW2 A/D conversion start request B
9Eh	—	GPTW3 compare match A
9Fh	—	GPTW3 compare match B
A0h	—	GPTW3 compare match C
A1h	—	GPTW3 compare match D
A2h	—	GPTW3 compare match E
A3h	—	GPTW3 compare match F
A4h	—	GPTW3 overflow
A5h	—	GPTW3 underflow
A6h	—	GPTW4 compare match A
A7h	—	GPTW4 compare match B
A8h	—	GPTW4 compare match C
A9h	—	GPTW4 compare match D
AAh	—	GPTW4 compare match E
ABh	—	GPTW4 compare match F
ACh	—	GPTW4 overflow
ADh	—	GPTW4 underflow
AEh	—	GPTW5 compare match A
AFh	—	GPTW5 compare match B
B0h	—	GPTW5 compare match C
B1h	—	GPTW5 compare match D
B2h	—	GPTW5 compare match E
B3h	—	GPTW5 compare match F
B4h	—	GPTW5 overflow
B5h	—	GPTW5 underflow
B6h	—	GPTW6 compare match A
B7h	—	GPTW6 compare match B
B8h	—	GPTW6 compare match C
B9h	—	GPTW6 compare match D
BAh	—	GPTW6 compare match E
BBh	—	GPTW6 compare match F
BCh	—	GPTW6 overflow
BDh	—	GPTW6 underflow
BEh	—	GPTW7 compare match A

Value of ELS[7:0] Bits	RX210 (ELC)	RX261 (ELC)
BFh	—	GPTW7 compare match B
C0h	—	GPTW7 compare match C
C1h	—	GPTW7 compare match D
C2h	—	GPTW7 compare match E
C3h	—	GPTW7 compare match F
C4h	—	GPTW7 overflow
C5h	—	GPTW7 underflow
C6h	—	GPTW (OPS) U-/V-/W-phase input edge detected

2.16 I/O Ports

Table 2.31 to Table 2.34 show a comparative overview of I/O ports, Table 2.35 shows a Comparison of I/O Port Functions, Table 2.36 shows a Comparison of Driving Ability Switching of I/O Ports, and Table 2.37 shows a Comparison of I/O Port Registers.

Table 2.31 Comparative Overview of I/O Ports (100-Pin)

Port Symbol	RX210 (100-Pin)	RX261 (100-Pin)
PORT0	P03, P05, P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTG	—	PG7
PORTH*1	PH0 to PH3	PH0, PH3, PH6, PH7
PORTJ	PJ1, PJ3	PJ1, PJ3, PJ6, PJ7

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.32 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX210 (80-Pin)	RX261 (80-Pin)
PORT0	P03, P05, P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20, P21, P26, P27	P20, P21, P26, P27
PORT3	P30 to P32, P34 to P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0 to PA6	PA0 to PA6
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC2 to PC7	PC0 to PC7
PORTD	PD0 to PD2	PD0 to PD2
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH*1	PH0 to PH3	PH0, PH3, PH6, PH7
PORTJ	PJ1	PJ1, PJ6, PJ7

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.33 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX210 (64-Pin)	RX261 (64-Pin)
PORT0	P03, P05	P03, P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P44, P46	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC2 to PC7	PC0 to PC7
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH*1	PH0 to PH3	PH0, PH3, PH6, PH7
PORTJ	—	PJ6, PJ7

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.34 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX210 (48-Pin)	RX261 (48-Pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P46	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC4 to PC7	PC0 to PC7
PORTE	PE1 to PE4	PE1 to PE4
PORTG	—	PG7
PORTH*1	PH0 to PH3	PH0, PH3
PORTJ	—	PJ6, PJ7

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.35 Comparison of I/O Port Functions

Item	Port Symbol	RX210	RX261
Input pull-up function	PORT0	P03, P05, P07	P03 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	P50 to P55
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTG	—	PG7
	PORTH*1	PH0 to PH3	PH0, PH3
	PORTJ	PJ1, PJ3	PJ1, PJ3, PJ6, PJ7
Open drain output function	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT5	—	P50 to P52, P54
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	—	PD0 to PD2
	PORTE	PE0 to PE7	PE0 to PE7
	PORTG	—	PG7
5V tolerance	PORT1	P12, P13, P16, P17	P12, P13, P16, P17

Note: 1. The RX260 devices have ports PH1 and PH2.

Table 2.36 Comparison of Driving Ability Switching of I/O Ports

Port Symbol	Driving Ability Switching	RX210	RX261
PORT0	Fixed to normal output	P03, P05, P07	—
	Normal drive/high drive	—	—
PORT1	Fixed to normal output	—	—
	Normal drive/high drive	P12 to P17	—
PORT2	Fixed to normal output	—	—
	Normal drive/high drive	P20 to P27	—
PORT3	Fixed to normal output	—	—
	Normal drive/high drive	P30 to P34, P36, P37	—
PORT4	Fixed to normal output	P40 to P47	—
	Normal drive/high drive	—	—
PORT5	Fixed to normal output	—	—
	Normal drive/high drive	P50 to P55	—
PORTA	Fixed to normal output	—	—
	Normal drive/high drive	PA0 to PA7	—
PORTB	Fixed to normal output	—	—
	Normal drive/high drive	PB0 to PB7	—
PORTC	Fixed to normal output	—	—
	Normal drive/high drive	PC0 to PC7	—

Port Symbol	Driving Ability Switching	RX210	RX261
PORTD	Fixed to normal output	—	—
	Normal drive/high drive	PD0 to PD7	—
PORTE	Fixed to normal output	—	—
	Normal drive/high drive	PE0 to PE7	—
PORTH	Fixed to normal output	—	—
	Normal drive/high drive	PH0 to PH3	—
PORTJ	Fixed to normal output	—	—
	Normal drive/high drive	PJ1, PJ3	—

Table 2.37 Comparison of I/O Port Registers

Register	Bit	RX210	RX261
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, G, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, G, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 bits (m = 0 to 5, A to E, G, H, J)
PMR	B0 to B6	Pm0 to Pm6 pin mode control bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm6 pin mode control bits (m = 0 to 5, A to E, G, H, J)
	B7	Pm7 pin mode control bit (m = 0 to 9, A to F, H, J to L) b7 0: Used as a general I/O port. 1: Used as peripheral function.	Pm7 pin mode control bit (m = 0 to 5, A to E, G, H, J) • PG7 b7 0: Used as a general I/O port. 1: Used as the MD function (initial value). • Others b7 0: Used as a general I/O port (initial value). 1: Used as peripheral function.
ODR0	B0, B4, B6	Pm0, Pm4, and Pm6 output type select bits (m = 0 to 3, 6 to 9, A to C, E, K)	Pm0, Pm4, and Pm6 output type select bits (m = 1 to 3, 5, A to E, J)
	B2, B3	Pm1 output type select bits (m = 0 to 3, 6 to 9, A to C, E, K) • P01, P21, P31, P51, P61, P81, P91, PA1, PB1, PC1 b2 0: CMOS output 1: N channel open drain b3 This bit is read as 0. The write value must be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N channel open drain 1 0: P channel open drain 1 1: Hi-Z	Pm1 output type select bits (m = 1 to 3, 5, A to E, J) • P21, P31, P51, PA1, PB1, PC1, PD1 b2 0: CMOS output 1: N channel open drain b3 This bit is read as 0. The write value must be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N channel open drain 1 0: P channel open drain 1 1: Prohibited

Register	Bit	RX210	RX261
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m =1 to 3, 7, A to C, E, K)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, 5, A to C, E, G)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, G, H, J)
PSRA	—	—	Port switching register A
PSRB	—	—	Port switching register B
PRWCNTR	—	—	Port reading wait control register
DSCR	—	Drive capacity control register	—

2.17 Multi-Function Pin Controller

Table 2.38 shows a Comparison of Multiplexed Pin Assignments, and Table 2.39 to Table 2.57 show comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **orange text** indicates pins that are present in the RX210 Group only, and **blue text** indicates pins that are present in the RX261 Group only. A circle (○) indicates that a function is assigned to the pin, a cross (×) indicates that the pin is not present or that no function is assigned, and grayed out items indicate functions that are not implemented.

Table 2.38 Comparison of Multiplexed Pin Assignments

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○	○	○
	IRQ0-DS (input)	P30	○	○	○	○				
	IRQ0 (input)	PD0	○	○	×	×	○	○	×	×
		PH1	○	○	○	○	○	○	○	○
		P30	×	×	×	×	○	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○				
	IRQ1 (input)	PD1	○	○	×	×	○	○	×	×
		PH2	○	○	○	○	○	○	○	○
		P31	×	×	×	×	○	○	○	○
	IRQ2-DS (input)	P32	○	○	○	×				
	IRQ2 (input)	P12	○	○	×	×	○	○	×	×
		PD2	○	○	×	×	○	○	×	×
		P32	×	×	×	×	○	○	○	×
		P36	×	×	×	×	○	○	○	○
	IRQ3-DS (input)	P33	○	×	×	×				
	IRQ3 (input)	P13	○	○	×	×	○	○	×	×
		PD3	○	×	×	×	○	×	×	×
		P33	×	×	×	×	○	×	×	×
	IRQ4-DS (input)	PB1	○	○	○	○				
	IRQ4 (input)	P14	○	○	○	○	○	○	○	○
		P34	○	○	×	×	○	○	×	×
		PD4	○	×	×	×	○	×	×	×
		P37	×	×	×	×	○	○	○	○
		PB1	×	×	×	×	○	○	○	○
	IRQ5-DS (input)	PA4	○	○	○	○				
	IRQ5 (input)	P15	○	○	○	○	○	○	○	○
		PD5	○	×	×	×	○	×	×	×
		PE5	○	○	○	×	○	○	○	×
		PA4	×	×	×	×	○	○	○	○
	IRQ6-DS (input)	PA3	○	○	○	○				
	IRQ6 (input)	P16	○	○	○	○	○	○	○	○
		PD6	○	×	×	×	○	×	×	×
		PE6	○	×	×	×	○	×	×	×
		PA3	×	×	×	×	○	○	○	○
	IRQ7-DS (input)	PE2	○	○	○	○				
	IRQ7 (input)	P17	○	○	○	○	○	○	○	○
		PD7	○	×	×	×	○	×	×	×
		PE7	○	×	×	×	○	×	×	×
		PE2	×	×	×	×	○	○	○	○

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	○	×	×				
		PB3	○	○	○	○				
	MTIOC0B (input/output)	P13	○	○	×	×				
		P15	○	○	○	○				
		PA1	○	○	○	○				
	MTIOC0C (input/output)	P32	○	○	○	×				
		PB1	○	○	○	○				
	MTIOC0D (input/output)	P33	○	×	×	×				
		PA3	○	○	○	○				
	MTIOC1A (input/output)	P20	○	○	×	×				
		PE4	○	○	○	○				
	MTIOC1B (input/output)	P21	○	○	×	×				
		PB5	○	○	○	○				
	MTIOC2A (input/output)	P26	○	○	○	○				
		PB5	○	○	○	○				
	MTIOC2B (input/output)	P27	○	○	○	○				
		PE5	○	○	○	×				
	MTIOC3A (input/output)	P14	○	○	○	○				
		P17	○	○	○	○				
		PC1	○	×	×	×				
		PC7	○	○	○	○				
		PJ1	○	○	×	×				
	MTIOC3B (input/output)	P17	○	○	○	○				
		P22	○	×	×	×				
		PB7	○	○	○	×				
		PC5	○	○	○	○				
	MTIOC3C (input/output)	P16	○	○	○	○				
		PC0	○	×	×	×				
		PC6	○	○	○	○				
		PJ3	○	×	×	×				
	MTIOC3D (input/output)	P16	○	○	○	○				
		P23	○	×	×	×				
		PB6	○	○	○	×				
		PC4	○	○	○	○				
	MTIOC4A (input/output)	P24	○	×	×	×				
		PA0	○	○	○	×				
		PB3	○	○	○	○				
		PE2	○	○	○	○				
	MTIOC4B (input/output)	P30	○	○	○	○				
		P54	○	○	○	×				
		PC2	○	○	○	×				
		PD1	○	○	×	×				
		PE3	○	○	○	○				
	MTIOC4C (input/output)	P25	○	×	×	×				
		PB1	○	○	○	○				
		PE1	○	○	○	○				
		PE5	○	○	○	×				

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC4D (input/output)	P31	○	○	○	○				
		P55	○	○	○	×				
		PC3	○	○	○	×				
		PD2	○	○	×	×				
		PE4	○	○	○	○				
	MTIC5U (input)	PA4	○	○	○	○				
		PD7	○	×	×	×				
	MTIC5V (input)	PA6	○	○	○	○				
		PD6	○	×	×	×				
	MTIC5W (input)	PB0	○	○	○	○				
		PD5	○	×	×	×				
	MTCLKA (input)	P14	○	○	○	○				
		P24	○	×	×	×				
		PA4	○	○	○	○				
		PC6	○	○	○	○				
	MTCLKB (input)	P15	○	○	○	○				
		P25	○	×	×	×				
		PA6	○	○	○	○				
		PC7	○	○	○	○				
	MTCLKC (input)	P22	○	×	×	×				
		PA1	○	○	○	○				
		PC4	○	○	○	○				
	MTCLKD (input)	P23	○	×	×	×				
		PA3	○	○	○	○				
		PC5	○	○	○	○				
Port output enable 2	POE0# (input)	PC4	○	○	○	○				
		PD7	○	×	×	×				
	POE1# (input)	PB5	○	○	○	○				
		PD6	○	×	×	×				
	POE2# (input)	P34	○	○	×	×				
		PA6	○	○	○	○				
		PD5	○	×	×	×				
	POE3# (input)	P33	○	×	×	×				
		PB3	○	○	○	○				
		PD4	○	×	×	×				
	POE8# (input)	P17	○	○	○	○				
		P30	○	○	○	○				
		PD3	○	×	×	×				
		PE3	○	○	○	○				
8-bit timer	TMO0 (output)	P22	○	×	×	×	○	×	×	×
		PB3	○	○	○	○	○	○	○	○
		PH1	○	○	○	○	○	○	○	○
	TMCI0 (input)	P21	○	○	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	○	○
		PH3	○	○	○	○	○	○	○	○
	TMRI0 (input)	P20	○	○	×	×	○	○	×	×
		PA4	○	○	○	○	○	○	○	○
		PH2	○	○	○	○	○	○	○	○

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
8-bit timer	TMO1 (output)	P17	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○
	TMCI1 (input)	P12	○	○	×	×	○	○	×	×
		P54	○	○	○	×	○	○	○	×
		PC4	○	○	○	○	○	○	○	○
	TMRI1 (input)	P24	○	×	×	×	○	×	×	×
		PB5	○	○	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○	○	○
		PC7	○	○	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○	○	○
		P31	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	×	×	○	○	×	×
		P32	○	○	○	×	○	○	○	×
		P55	○	○	○	×	○	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	○	○	○
		P34	○	○	×	×	○	○	×	×
		PA6	○	○	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○	○	○
		P33	○	×	×	×	○	×	×	×
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○*3	×	×				
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	○*3	×	×				
	SCK0 (input/output)	P22	○	×	×	×				
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	×	×	×				
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○	○	○
		P30	○	○	○	○	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○	○	○
		P27	○	○	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○	○	○
		P31	○	○	○	○	○	○	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○	×	×	○	○	×	×
		PA3	○	○	○	○	○	○	○	○
		PC2	○	○	○	×	○	○	○	×
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○	○	○	○	○	○	○
		PC3	○	○	○	×	○	○	○	×

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	SCK5 (input/output)	PA1	○	○	○	○	○	○	○	○
		PC1	○	×	×	×	○	×	×	×
		PC4	○	○	○	○	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○	○	○
		PC0	○	×	×	×	○	×	×	×
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P33	○	×	×	×	○	×	×	×
		PB0	○	○	○	○	○	○	○	○
		PD1	×	×	×	×	○	○	×	×
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P32	○	○	○	×	○	○	○	×
		PB1	○	○	○	○	○	○	○	○
		PD0	×	×	×	×	○	○	×	×
	SCK6 (input/output)	P34	○	○	×	×	○	○	×	×
		PB3	○	○	○	○	○	○	○	○
		PD2	×	×	×	×	○	○	×	×
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	○	×	×	○	○	×	×
		PJ3	○	×	×	×	○	×	×	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○				
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○	○				
	SCK8 (input/output)	PC5	○	○	○	○				
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○	○				
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○	×				
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	○	×				
	SCK9 (input/output)	PB5	○	○	○	×				
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	PB4	○	○	×	×				
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	○	○	○	○*4	○	○	○	○*4
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○	○	○*5	○	○	○	○*5
	SCK12 (input/output)	PE0	○	○	○	×	○	○	○	×
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○	○*6	○	○	○	○*6

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD000 (input)/ SMISO000 (input/output)/ SSCL000 (input/output)	P21					○	○	×	×
	TXD000 (output)/ TXDA000 (output)/ SMOSI000 (input/output)/ SSDA000 (input/output)	P20					○	○*7	×	×
	SCK000 (input/output)	P22					○	×	×	×
	TXDB000 (output)	P22					○	×	×	×
	CTS000# (input)/ RTS000# (output)/ SS000# (input)	P23					○	×	×	×
	DE000 (output)	P23					○	×	×	×
	RXD008 (input)/ SMISO008 (input/output)/ SSCL008 (input/output)	PC6					○	○	○	○
	TXD008 (output)/ TXDA008 (output)/ SMOSI008 (input/output)/ SSDA008 (input/output)	PC7					○	○	○	○
	SCK008 (input/output)	PC5					○	○	○	○
	TXDB008 (output)	PC5					○	○	○	○
	CTS008# (input)/ RTS008# (output)/ SS008# (input)	PC4					○	○	○	○
	DE008 (output)	PC4					○	○	○	○
	RXD009 (input)/ SMISO009 (input/output)/ SSCL009 (input/output)	PB6					○	○	○	×
	TXD009 (output)/ TXDA009 (output)/ SMOSI009 (input/output)/ SSDA009 (input/output)	PB7					○	○	○	×
	SCK009 (input/output)	PB5					○	○	○	×
	TXDB009 (output)	PB5					○	○	○	×
	CTS009# (input)/ RTS009# (output)/ SS009# (input)	PB4					○	○	×	×
	DE009 (output)	PB4					○	○	×	×
I^2C bus interface	SCL-DS (input/output)	P16	○	○	○	○				
	SCL (input/output)	P12	○	○	×	×				
	SDA-DS (input/output)	P17	○	○	○	○				
	SDA (input/output)	P13	○	○	×	×				
	SCL0 (input/output)	P12					○	○	×	×
		P16					○	○	○	○
	SDA0 (input/output)	P13					○	○	×	×
		P17					○	○	○	○
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	×	×	○	○	×	×
		PB0	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial peripheral interface	MOSIA (input/output)	P16	○	○	○	○	○	○	○	○
		PA6	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○	○	○
		PA7	○	×	×	×	○	×	×	×
		PC7	○	○	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○	○	○
		PC4	○	○	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	○	×	○	○	○	×
		PC0	○	×	×	×	○	×	×	×
	SSLA2 (output)	PA1	○	○	○	○	○	○	○	○
		PC1	○	×	×	×	○	×	×	×
	SSLA3 (output)	PA2	○	○	×	×	○	○	×	×
		PC2	○	○	○	×	○	○	○	×
Realtime clock	RTCOUT (output)	P16	○	○	○	×	○	○	○	×
		P32	○	○	○	×	○	○	○	×
	RTCIC0 (input)*1	P30	○	○	○	×	○	○	○	×
	RTCIC1 (input)*1	P31	○	○	○	×	○	○	○	×
	RTCIC2 (input)*1	P32	○	○	○	×	○	○	○	×
12-bit A/D converter	AN000 (input)*1	P40	○	○	○	○	○	○	○	○
	AN001 (input)*1	P41	○	○	○	○	○	○	○	○
	AN002 (input)*1	P42	○	○	○	○	○	○	○	○
	AN003 (input)*1	P43	○	○	○	×	○	○	○	×
	AN004 (input)*1	P44	○	○	○	×	○	○	○	×
	AN005 (input)*1	P45	○	○	×	×	○	○	○	○
	AN006 (input)*1	P46	○	○	○	○	○	○	○	○
	AN007 (input)*1	P47	○	○	×	×	○	○	○	○
	AN008 (input)*1	PE0	○	○	○	×				
	AN009 (input)*1	PE1	○	○	○	○				
	AN010 (input)*1	PE2	○	○	○	○				
	AN011 (input)*1	PE3	○	○	○	○				
	AN012 (input)*1	PE4	○	○	○	○				
	AN013 (input)*1	PE5	○	○	○	×				
	AN014 (input)*1	PE6	○	×	×	×				
	AN015 (input)*1	PE7	○	×	×	×				
	AN016 (input)*1	PE0					○	○	○	×
	AN017 (input)*1	PE1					○	○	○	○
	AN018 (input)*1	PE2					○	○	○	○
	AN019 (input)*1	PE3					○	○	○	○
	AN020 (input)*1	PE4					○	○	○	○
	AN021 (input)*1	PE5					○	○	○	×
	AN022 (input)*1	PE6					○	×	×	×
	AN023 (input)*1	PE7					○	×	×	×
	AN024 (input)*1	PD0					○	○	×	×
	AN025 (input)*1	PD1					○	○	×	×
	AN026 (input)*1	PD2					○	○	×	×
	AN027 (input)*1	PD3					○	×	×	×
	AN028 (input)*1	PD4					○	×	×	×
	AN029 (input)*1	PD5					○	×	×	×

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
12-bit A/D converter	AN030 (input)*1	PD6					○	×	×	×
	AN031 (input)*1	PD7					○	×	×	×
	ADTRG0# (input)	P07	○	○	×	×	○	○	×	×
		P16	○	○	○	○	○	○	○	○
		P25	○	×	×	×	○	×	×	×
D/A converter	DA0 (output) *1	P03	○	○	○	×	○	○	○	×
	DA1 (output) *1	P05	○	○	○	×	○	○	○	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	○	×	○	○	○	×
		PC7	○	○	○	○	○	○	○	○
		PH0	○	○	○	○	○	○	○	○
Comparator A	CMPA1 (input)*1	PE3	○	○	○	○				
	CMPA2 (input)*1	PE4	○	○	○	○				
	CVREFA (input)*1	PA1	○	○	○	○				
Comparator B	CMPB0 (input)*1	PE1	○	○	○	○	○	○	○	○
	CVREFB0 (input)*1	PE2	○	○	○	○	○	○	○	○
	CMPOB0 (output)	PE5					○	○	○	×
	CMPB1 (input)*1	PA3	○	○	○	○	○	○	○	○
	CVREFB1 (input)*1	PA4	○	○	○	○	○	○	○	○
	CMPOB1 (output)	PB1					○	○	○	○
External bus	CS0# (output)	P24	○	×	×	×				
		PC7	○	×	×	×				
	CS1# (output)	P25	○	×	×	×				
		PC6	○	×	×	×				
	CS2# (output)	P26	○	×	×	×				
		PC5	○	×	×	×				
	CS3# (output)	P27	○	×	×	×				
		PC4	○	×	×	×				
	A0 to A7 (output)	PA0 to PA7	○	×	×	×				
	A8 to A15 (output)	PB0 to PB7	○	×	×	×				
	A16 to A23 (output)	PC0 to PC7	○	×	×	×				
	D0 to D7 (input/output)	PD0 to PD7	○	×	×	×				
	D8 to D15 (input/output)	PE0 to PE7	○	×	×	×				
	BCLK (output)	P53	○	×	×	×				
	RD# (output)	P52	○	×	×	×				
	WR# (output)	P50	○	×	×	×				
	WR0# (output)	P50	○	×	×	×				
	WR1# (output)	P51	○	×	×	×				
	BC0# (output)	PA0	○	×	×	×				
	BC1# (output)	P51	○	×	×	×				
	WAIT# (input)	P51	○	×	×	×				
		P55	○	×	×	×				
		PC5	○	×	×	×				
	ALE (output)	P54	○	×	×	×				
Clock generation circuit	CLKOUT (output)	PE3					○	○	○	○
		PE4					○	○	○	○

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P17					○	○	○	○
		P22					○	×	×	×
		PA0					○	○	○	×
		PA1					○	○	○	○
		PB7					○	○	○	×
		PC5					○	○	○	○
		PH0					○	○	○	○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P16					○	○	○	○
		P17					○	○	○	○
		P23					○	×	×	×
		PA1					○	○	○	○
		PA6					○	○	○	○
		PB0					○	○	○	○
		PB6					○	○	○	×
		PC4					○	○	○	○
		PH1					○	○	○	○
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P24					○	×	×	×
		P32					○	○	○	×
		P55					○	○	○	×
		PA0					○	○	○	×
		PB3					○	○	○	○
		PE2					○	○	○	○
		PE4					○	○	○	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P25					○	×	×	×
		P33					○	×	×	×
		PA3					○	○	○	○
		PA4					○	○	○	○
		PB1					○	○	○	○
		PE1					○	○	○	○
		PE5					○	○	○	×
		PH2					○	○	○	○
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P21					○	○	×	×
		P30					○	○	○	○
		P54					○	○	○	×
		PB0					○	○	○	○
		PC2					○	○	○	×
		PD1					○	○	×	×
		PE3					○	○	○	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P20					○	○	×	×
		P31					○	○	○	○
		P55					○	○	○	×
		PA3					○	○	○	○
		PB1					○	○	○	○
		PC3					○	○	○	×
		PD2					○	○	×	×
		PE4					○	○	○	○
		PH3					○	○	○	○

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTIOC3A (input/output)/ GTIOC3A# (input/output)	P22					○	×	×	×
		P34					○	○	×	×
		PB2					○	○	×	×
		PB3					○	○	○	○
		PC4					○	○	○	○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	P13					○	○	×	×
		P15					○	○	○	○
		P23					○	×	×	×
		PA1					○	○	○	○
		PB3					○	○	○	○
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P20					○	○	×	×
		PA4					○	○	○	○
		PE4					○	○	○	○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P16					○	○	○	○
		P21					○	○	×	×
		PA5					○	○	×	×
		PB5					○	○	○	○
		PE3					○	○	○	○
	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P26					○	○	○	○
		PA6					○	○	○	○
		PB5					○	○	○	○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P15					○	○	○	○
		P27					○	○	○	○
		PA7					○	×	×	×
		PE5					○	○	○	×
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P14					○	○	○	○
		P17					○	○	○	○
		P25					○	×	×	×
		PB4					○	○	×	×
		PC1					○	×	×	×
		PC7					○	○	○	○
		PJ1					○	○	×	×
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P16					○	○	○	○
		P24					○	×	×	×
		PB5					○	○	○	○
		PC0					○	×	×	×
		PC6					○	○	○	○
		PJ3					○	×	×	×
	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P13					○	○	×	×
		P32					○	○	○	×
		PB1					○	○	○	○
		PB6					○	○	○	×
		PC5					○	○	○	○

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P14					○	○	○	○
		P33					○	×	×	×
		PA3					○	○	○	○
		PB7					○	○	○	×
	GTETRGA (input)	P14					○	○	○	○
		P24					○	×	×	×
		PA4					○	○	○	○
		PC2					○	○	○	×
		PC6					○	○	○	○
	GTETRGB (input)	P15					○	○	○	○
		P25					○	×	×	×
		PA3					○	○	○	○
		PA6					○	○	○	○
		PC3					○	○	○	×
		PC7					○	○	○	○
	GTETRGC (input)	P16					○	○	○	○
		P22					○	×	×	×
		PA1					○	○	○	○
		PB2					○	○	×	×
		PC0					○	×	×	×
		PC4					○	○	○	○
	GTETRGD (input)	P17					○	○	○	○
		P23					○	×	×	×
		PA3					○	○	○	○
		PB3					○	○	○	○
		PC1					○	×	×	×
		PC5					○	○	○	○
	GTCPPO0 (output)	P14					○	○	○	○
		P17					○	○	○	○
		PC1					○	×	×	×
		PC7					○	○	○	○
		PJ1					○	○	×	×
	GTIU (input)	P34					○	○	×	×
		PB3					○	○	○	○
		PC4					○	○	○	○
	GTIV (input)	P13					○	○	×	×
		P15					○	○	○	○
		PA1					○	○	○	○
	GTIW (input)	P32					○	○	○	×
		PB1					○	○	○	○
		PC5					○	○	○	○
	GTOULO (output)	P16					○	○	○	○
		PA6					○	○	○	○
		PC4					○	○	○	○
		PH1					○	○	○	○
	GTOUUP (output)	P17					○	○	○	○
		PA1					○	○	○	○
		PC5					○	○	○	○
		PH0					○	○	○	○

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTOVLO (output)	PA3					○	○	○	○
		PA4					○	○	○	○
		PB1					○	○	○	○
		PE1					○	○	○	○
	GTOVUP (output)	PA0					○	○	○	×
		PB3					○	○	○	○
		PE2					○	○	○	○
		PE4					○	○	○	○
	GTOWLO (output)	P31					○	○	○	○
		PA3					○	○	○	○
		PB1					○	○	○	○
		PE4					○	○	○	○
	GTOWUP (output)	P30					○	○	○	○
		PB0					○	○	○	○
		PC2					○	○	○	×
		PE3					○	○	○	○
Low power timer	LPTO (output)	P26					○	○	○	○
		PB3					○	○	○	○
		PC7					○	○	○	○
CANFD module	CTX0 (output)	P14					○	○	○	○
		P32					○	○	○	×
		P54					○	○	○	×
		PD1					○	○	×	×
	CRX0 (input)	P15					○	○	○	○
		P33					○	×	×	×
		P55					○	○	○	×
		PD2					○	○	×	×
USB 2.0 FS host/function module	USB0_DP (input/output)	PH1*2					○	○	○	○
	USB0_DM (input/output)	PH2*2					○	○	○	○
	USB0_VBUS (input)	P16					○	○	○	○
		PB5					○	○	○	○
	USB0_EXICEN (output)	P21					○	○	×	×
		PC6					○	○	○	○
	USB0_VBUSEN (output)	P16					○	○	○	○
		P24					○	×	×	×
		P26					○	○	○	○
		P32					○	○	○	×
	USB0_OVRCURA (input)	P14					○	○	○	○
	USB0_OVRCURB (input)	P16					○	○	○	○
		P22					○	×	×	×
	USB0_ID (input)	P20					○	○	×	×
		PC5					○	○	○	○
LVD voltage detection input	CMPA2 (input)*1	PE4					○	○	○	○
Capacitive touch sensing unit (CTSU)	TSCAP (—)	PC4					○	○	○	○
	TS0 (input/output)	P32					○	○	○	×
	TS1 (input/output)	P31					○	○	○	○
	TS2 (output)	P30					○	○	○	○
	TS3 (output)	P27					○	○	○	○

Module Function	Pin Function	Port Allocation	RX210				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Capacitive touch sensing unit (CTSU)	TS4 (output)	P26					○	○	○	○
	TS5 (output)	P15					○	○	○	○
	TS6 (output)	P14					○	○	○	○
	TS7 (output)	PH3					○	○	○	○
	TS8 (output)	PH2					○	○	○	○
	TS9 (output)	PH1					○	○	○	○
	TS10 (output)	PH0					○	○	○	○
	TS11 (output)	P55					○	○	○	×
	TS12 (output)	P54					○	○	○	×
	TS13 (output)	PC7					○	○	○	○
	TS14 (output)	PC6					○	○	○	○
	TS15 (output)	PC5					○	○	○	○
	TS16 (output)	PC3					○	○	○	×
	TS17 (output)	PC2					○	○	○	×
	TS18 (output)	PB7					○	○	○	×
	TS19 (output)	PB6					○	○	○	×
	TS20 (output)	PB5					○	○	○	○
	TS21 (output)	PB4					○	○	×	×
	TS22 (output)	PB3					○	○	○	○
	TS23 (output)	PB2					○	○	×	×
	TS24 (output)	PB1					○	○	○	○
	TS25 (output)	PB0					○	○	○	○
	TS26 (output)	PA6					○	○	○	○
	TS27 (output)	PA5					○	○	×	×
	TS28 (output)	PA4					○	○	○	○
	TS29 (output)	PA3					○	○	○	○
	TS30 (output)	PA2					○	○	×	×
	TS31 (output)	PA1					○	○	○	○
	TS32 (output)	PA0					○	○	○	×
	TS33 (output)	PE4					○	○	○	○
	TS34 (output)	PE3					○	○	○	○
	TS35 (output)	PE2					○	○	○	○
Remote control signal receiver	PMC0 (input)	P51					○	×	×	×
		P53					○	×	×	×
		PB3					○	○	○	○
		PC3					○	○	○	×
		PC4					○	○	○	○
		PC5					○	○	○	○

Notes: 1. To use this pin function, select general input by setting the PORT.PDR.Bm bit and PORT.PMR.Bm bit for the applicable pin to 0.
2. Pins PH1 and PH2 for RX260 Group products. Pins USB0_DP and USB0_DM for RX261 Group products.
3. SMISO0 function is not available.
4. SMISO12 function is not available.
5. SMOSI12 function is not available.
6. SS12# function is not available.
7. TXDA000 function is not available.

Table 2.39 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX210 (n = 0 to 3, 5, 7)	RX261 (n = 3, 5, 7)
P00PFS	PSEL[3:0]	Pin function select bits	—
P01PFS	PSEL[3:0]	Pin function select bits	—
P02PFS	PSEL[3:0]	Pin function select bits	—

Table 2.40 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX210 (n = 2 to 7)	RX261 (n = 2 to 7)
P12PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0101b: TMCI1 1010b: RXD2/SMISO2/SSCL2 1111b: SCL	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 01111b: SCL0
P13PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0B 0011b: TIOCA5 0101b: TMO3 1010b: TXD2/SMOSI2/SSDA2 1111b: SDA	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTIV 00101b: TMO3 01111b: SDA0 10100b: GTIOC3B 10101b: GTIOC7A 10110b: GTIOC3B# 10111b: GTIOC7A#
P14PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTCLKA 0011b: TIOCB5 0100b: TCLKA 0101b: TMRI2 1011b: CTS1#/RTS1#/SS1#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTCPPO0 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 10000b: CTX0 10001b: USB0_OVRCURA 10100b: GTIOC6A 10101b: GTIOC7B 10110b: GTIOC6A# 10111b: GTIOC7B# 11000b: GTETRGA 11001b: TS6

Register	Bit	RX210 (n = 2 to 7)	RX261 (n = 2 to 7)
P15PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0B 0010b: MTCLKB 0011b: TIOCB2 0100b: TCLKB 0101b: TMCI2 1010b: RXD1/SMISO1/SSCL1 1011b: SCK3	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTIV 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 10000b: CRX0 10100b: GTIOC3B 10101b: GTIOC5B 10110b: GTIOC3B# 10111b: GTIOC5B# 11000b: GTETRGB 11001b: TS5
P16PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3C 0010b: MTIOC3D 0011b: TIOCB1 0100b: TCLKC 0101b: TMO2 0111b: RTCOUT 1001b: ADTRG0# 1010b: TXD1/SMOSI1/SSDA1 1011b: RXD3/SMISO3/SSCL3 1101b: MOSIA 1111b: SCL-DS	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC6B# 00010b: GTETRGC 00011b: GTOULO 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL0 10001b: USB0_VBUS 10010b: USB0_VBUSEN 10011b: USB0_OVRCURB 10100b: GTIOC0B 10101b: GTIOC4B 10110b: GTIOC0B# 10111b: GTIOC4B# 11000b: GTIOC6B

Register	Bit	RX210 (n = 2 to 7)	RX261 (n = 2 to 7)
P17PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTIOC3B 0011b: TIOCB0 0100b: TCLKD 0101b: TMO1 0111b: POE8# 1010b: SCK1 1011b: TXD3/SMOSI3/SSDA3 1101b: MISOA 1111b: SDA-DS	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC6A# 00010b: GTETRGD 00011b: GTCPPO0 00100b: GTOUUP 00101b: TMO1 01010b: SCK1 01101b: MISOA 01111b: SDA0 10100b: GTIOC0A 10101b: GTIOC0B 10110b: GTIOC0A# 10111b: GTIOC0B# 11000b: GTIOC6A

Table 2.41 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
P20PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC1A 0011b: TIOCB3 0101b: TMRI0 0101b: TXD0/SMOSI0/SSDA0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 01010b: TXD000/TXDA000/ SMOSI000/SSDA000 10001b: USB0_ID 10100b: GTIOC2B 10101b: GTIOC4A 10110b: GTIOC2B# 10111b: GTIOC4A#
P21PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC1B 0011b: TIOCA3 0101b: TMCI0 1010b: RXD0/SMISO0/SSCL0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 01010b: RXD000/SMISO000/ SSCL000 10001b: USB0_EXICEN 10100b: GTIOC2A 10101b: GTIOC4B 10110b: GTIOC2A# 10111b: GTIOC4B#
P22PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3B 0010b: MTCLKC 0011b: TIOCC3 0101b: TMO0 1010b: SCK0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: SCK000 01100b: TXDB000 10001b: USB0_OVRCURB 10100b: GTIOC0A 10101b: GTIOC3A 10110b: GTIOC0A# 10111b: GTIOC3A# 11000b: GTETRGC

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
P23PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3D 0010b: MTCLKD 0011b: TIOCD3 1010b: TXD3/SMOSI3/SSDA3 1011b: CTS0#/RTS#/SS0#	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS000#/RTS000#/ SS000# 01100b: DE000 10100b: GTIOC0B 10101b: GTIOC3B 10110b: GTIOC0B# 10111b: GTIOC3B# 11000b: GTETRGD
P24PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4A 0010b: MTCLKA 0011b: TIOCB4 0101b: TMRI1 1010b: SCK3	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI1 10001b: USB0_VBUSEN 10100b: GTIOC1A 10101b: GTIOC6B 10110b: GTIOC1A# 10111b: GTIOC6B# 11000b: GTETRGA
P25PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4C 0010b: MTCLKB 0011b: TIOCA4 1001b: ADTRG0# 1010b: RXD3/SMISO3/SSCL3	Pin function select bits b4 b0 00000b: Hi-Z 01001b: ADTRG0# 10100b: GTIOC1B 10101b: GTIOC6A 10110b: GTIOCIB# 10111b: GTIOC6A# 11000b: GTETRGB

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
P26PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC2A 0101b: TMO1 1010b: TXD1/SMOSI1/SSDA1 1011b: CTS3#/RTS3#/SS3#	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 10001b: USB0_VBUSEN 10100b: GTIOC5A 10110b: GTIOC5A# 11001b: TS4 11011b: LPTO
P27PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC2B 0101b: TMCI3 1010b: SCK1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI3 01010b: SCK1 10100b: GTIOC5B 10110b: GTIOC5B# 11001b: TS3

Table 2.42 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX210 (n = 0 to 4)	RX261 (n = 0 to 4, 6, 7)
P30PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4B 0101b: TMRI3 0111b: POE8# 1010b: RXD1/SMISO1/SSCL1	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWUP 00101b: TMRI3 01010b: RXD1/SMISO1/SSCL1 10100b: GTIOC2A 10110b: GTIOC2A# 11001b: TS2
P31PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4D 0101b: TMCI2 1011b: CTS1#/RTS1#/SS1#	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWLO 00101b: TMCI2 01011b: CTS1#/RTS1#/SS1# 10100b: GTIOC2B 10110b: GTIOC2B# 11001b: TS1
P32PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0C 0011b: TIOCC0 0101b: TMO3 0111b: RTCOUT 1010b: TXD0/SMOSI0/SSDA0 1011b: TXD6/SMOSI6/SSDA6	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTIW 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 10000b: CTX0 10001b: USB0_VBUSEN 10100b: GTIOC1A 10101b: GTIOC7A 10110b: GTIOC1A# 10111b: GTIOC7A# 11001b: TS0

Register	Bit	RX210 (n = 0 to 4)	RX261 (n = 0 to 4, 6, 7)
P33PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0D 0011b: TIOCD0 0101b: TMRI3 0111b: POE3# 1010b: RXD0/SMISO0/SSCL0 1011b: RXD6/SMISO6/SSCL6	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI3 01011b: RXD6/SMISO6/SSCL6 10000b: CRX0 10100b: GTIOC1B 10101b: GTIOC7B 10110b: GTIOC1B# 10111b: GTIOC7B#
P34PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0A 0101b: TMCI3 0111b: POE2# 1010b: SCK0 1011b: SCK6	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIU 00101b: TMCI3 01011b: SCK6 10100b: GTIOC3A 10110b: GTIOC3A#
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (145/144/100/80/69/64/48-pin) P31: IRQ1-DS (145/144/100/80/69/64/48-pin) P32: IRQ2-DS (145/144/100/80/69/64-pin) P33: IRQ3-DS (145/144/100-pin) P34: IRQ4 (145/144/100/80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (100/80/64/48-pin) P31: IRQ1 (100/80/64/48-pin) P32: IRQ2 (100/80/64-pin) P33: IRQ3 (100-pin) P34: IRQ4 (100/80-pin) P36: IRQ2 (80/64/48-pin) P37: IRQ4 (80/64/48-pin)

Table 2.43 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX210 (n = 0 to 2, 4 to 6)	RX261 (n = 1, 3 to 5)
P50PFS	PSEL[3:0]	Pin function select bits	—
P51PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 1010b: SCK2	Pin function select bits b4 b0 00000b: Hi-Z 11100b: PMC0
P52PFS	PSEL[3:0]	Pin function select bits	—

Register	Bit	RX210 (n = 0 to 2, 4 to 6)	RX261 (n = 1, 3 to 5)
P53PFS	PSEL[4:0]	—	Pin function select bits
P54PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4B 0101b: TMCI1 1011b: CTS2#/RTS2#/SS2#	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 10000b: CTX0 10100b: GTIOC2A 10110b: GTIOC2A# 11001b: TS12
P55PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4D 0101b: TMO3	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO3 10000b: CRX0 10100b: GTIOC1A 10101b: GTIOC2B 10110b: GTIOC1A# 10111b: GTIOC2B# 11001b: TS11
P56PFS	PSEL[3:0]	Pin function select bits	—

Table 2.44 Comparison of P6n Pin Function Control Register (P6nPFS)

Register	Bit	RX210 (n = 0, 1)	RX261
P6nPFS	—	P6n pin function control register	—

Table 2.45 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX210 (n = 0, 4 to 7)	RX261
P7nPFS	—	P7n pin function control register	—

Table 2.46 Comparison of P8n Pin Function Control Register (P8nPFS)

Register	Bit	RX210 (n = 0 to 3, 6, 7)	RX261
P8nPFS	—	P8n pin function control register	—

Table 2.47 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX210 (n = 0 to 3)	RX261
P9nPFS	—	P9n pin function control register	—

Table 2.48 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PA0PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4A 0011b: TIOCA0 0111b: CACREF 1101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOVUP 00111b: CACREF 01101b: SSLA1 10100b: GTIOC0A 10101b: GTIOC1A 10110b: GTIOC0A# 10111b: GTIOC1A# 11001b: TS32
PA1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0B 0010b: MTCLKC 0011b: TIOCB0 1010b: SCK5 1101b: SSLA2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC3B# 00010b: GTETRGC 00011b: GTIV 00100b: GTOUUP 01010b: SCK5 01101b: SSLA2 10100b: GTIOC0A 10101b: GTIOC0B 10110b: GTIOC0A# 10111b: GTIOC0B# 11000b: GTIOC3B 11001b: TS31
PA2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 1010b: RXD5/SMISO5/SSCL5 1101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS30

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PA3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0D 0010b: MTCLKD 0011b: TIOCD0 0100b: TCLKB 1010b: RXD5/SMISO5/SSCL5	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC7B# 00010b: GTETRGB 00011b: GTETRGD 00100b: GTOVLO 01000b: GTOWLO 01010b: RXD5/SMISO5/SSCL5 10100b: GTIOC1B 10101b: GTIOC2B 10110b: GTIOC1B# 10111b: GTIOC2B# 11000b: GTIOC7B 11001b: TS29
PA4PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIC5U 0010b: MTCLKA 0011b: TIOCA1 0101b: TMRI0 1010b: TXD5/SMOSI5/SSDA5 1101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOVLO 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 10100b: GTIOC1B 10101b: GTIOC4A 10110b: GTIOC1B# 10111b: GTIOC4A# 11000b: GTETRGA 11001b: TS28
PA5PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0011b: TIOCB1 1101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 01101b: RSPCKA 10100b: GTIOC4B 10110b: GTIOC4B# 11001b: TS27

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PA6PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIC5V 0010b: MTCLKB 0011b: TIOCA2 0101b: TMCI3 0111b: POE2# 1011b: CTS5#/RTS5#/SS5# 1101b: MOSIA	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOULO 00101b: TMCI3 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 10100b: GTIOC0B 10101b: GTIOC5A 10110b: GTIOC0B# 10111b: GTIOC5A# 11000b: GTETRGB 11001b: TS26
PA7PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0011b: TIOCB2 1101b: MISOA	Pin function select bits b4 b0 00000b: Hi-Z 01101b: MISOA 10100b: GTIOC5B 10110b: GTIOC5B#
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6-DS (145/144/100/80/69/64/48-pin) PA4: IRQ5-DS (145/144/100/80/69/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 (100/80/64/48-pin) PA4: IRQ5 (100/80/64/48-pin)
PAnPFS	ASEL	Analog function select bit 0: Used as other than an analog pin. 1: Used as an analog pin. PA1: CVREFA (145/144/100/80/69/64/48-pin) PA3: CMPB1 (145/144/100/80/69/64/48-pin) PA4: CVREFB1 (145/144/100/80/69/64/48-pin)	Analog function select bit 0: Used as other than an analog pin. 1: Used as an analog pin. PA3: CMPB1 (100/80/64/48-pin) PA4: CVREFB1 (100/80/64/48-pin)

Table 2.49 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PB0PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIC5W 0011b: TIOCA3 1010b: RXD4/SMISO4/SSCL4 1011b: RXD6/SMISO6/SSCL6 1101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWUP 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 10100b: GTIOC0B 10101b: GTIOC2A 10110b: GTIOC0B# 10111b: GTIOC2A# 11001b: TS25
PB1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0C 0010b: MTIOC4C 0011b: TIOCB3 0101b: TMCI0 1010b: TXD4/SMOSI4/SSDA4 1011b: TXD6/SMOSI6/SSDA6	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC7A# 00010b: GTOVLO 00011b: GTIW 00100b: GTOWLO 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 10100b: GTIOC1B 10101b: GTIOC2B 10110b: GTIOC1B# 10111b: GTIOC2B# 11000b: GTIOC7A 11001b: TS24
PB2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0011b: TIOCC3 0100b: TCLKC 1010b: CTS4#/RTS4#/SS4# 1011b: CTS6#/RTS6#/SS6#	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 10100b: GTIOC3A 10110b: GTIOC3A# 11000b: GTETRGC 11001b: TS23

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PB3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC0A 0010b: MTIOC4A 0011b: TIOCD3 0100b: TCLKD 0101b: TMO0 0111b: POE3# 1010b: SCK4 1011b: SCK6	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC3B# 00010b: GTETRGD 00011b: GTIU 00100b: GTOVUP 00101b: TMO0 01011b: SCK6 10100b: GTIOC1A 10101b: GTIOC3A 10110b: GTIOC1A# 10111b: GTIOC3A# 11000b: GTIOC3B 11001b: TS22 11011b: LPTO 11100b: PMC0
PB4PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0011b: TIOCA4 1011b: CTS9#/RTS9#/SS9#	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS009#/RTS009#/ SS009# 01100b: DE009 10100b: GTIOC6A 10110b: GTIOC6A# 11001b: TS21
PB5PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC2A 0010b: MTIOC1B 0011b: TIOCB4 0101b: TMRI1 0111b: POE1# 1010b: SCK9	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC6B# 00101b: TMRI1 01010b: SCK009 01100b: TXDB009 10001b: USB0_VBUS 10100b: GTIOC4B 10101b: GTIOC5A 10110b: GTIOC4B# 10111b: GTIOC5A# 11000b: GTIOC6B 11001b: TS20

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PB6PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3D 0011b: TIOCA5 1010b: RXD9/SMISO9/SSCL9	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD009/SMISO009/ SSCL009 10100b: GTIOC0B 10101b: GTIOC7A 10110b: GTIOC0B# 10111b: GTIOC7A# 11001b: TS19
PB7PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3B 0011b: TIOCB5 1010b: TXD9/SMOSI9/SSDA9	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD009/TXDA009/ SMOSI009/SSDA009 10100b: GTIOC0A 10101b: GTIOC7B 10110b: GTIOC0A# 10111b: GTIOC7B# 11101b: TS18
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4-DS (145/144/100/80/69/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/80/64/48-pin)

Table 2.50 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PC0PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3C 0011b: TCLKC 1011b: CTS5#/RTS5#/SS5# 1101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS5#/RTS5#/SS5# 01101b: SSLA1 10100b: GTIOC6B 10110b: GTIOC6B# 11000b: GTETRGC

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PC1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3A 0011b: TCLKD 1010b: SCK5 1101b: SSLA2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTCPPO0 01010b: SCK5 01101b: SSLA2 10110b: GTIOC6A 10110b: GTIOC6A# 11000b: GTETRGD
PC2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4B 0011b: TCLKA 1010b: RXD5/SMISO5/SSCL5 1101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWUP 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 10100b: GTIOC2A 10110b: GTIOC2A# 11000b: GTETRGA 11001b: TS17
PC3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4D 0011b: TCLKB 1010b: TXD5/SMOSI5/SSDA5	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/SMOSI5/SSDA5 10100b: GTIOC2B 10110b: GTIOC2B# 11000b: GTETRGB 11001b: TS16 11100b: PMC0

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PC4PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3D 0010b: MTCLKC 0101b: TMCI1 0111b: POE0# 1010b: SCK5 1011b: CTS8#/RTS8#/SS8# 1101b: SSLA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIU 00011b: GTOULO 00101b: TMCI1 01010b: SCK5 01011b: CTS008#/RTS008#/ SS008# 01100b: DE008 01101b: SSLA0 10100b: GTIOC0B 10101b: GTIOC3A 10110b: GTIOC0B# 10111b: GTIOC3A# 11000b: GTETRGC 11001b: TSCAP 11100b: PMC0
PC5PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3B 0010b: MTCLKD 0101b: TMRI2 1010b: SCK8 1101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOUUP 00011b: GTIW 00101b: TMRI2 01010b: SCK008 01100b: TXDB008 01101b: RSPCKA 10001b: USB0_ID 10100b: GTIOC0A 10101b: GTIOC7A 10110b: GTIOC0A# 10111b: GTIOC7A# 11000b: GTETRGD 11001b: TS15 11100b: PMC0

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PC6PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3C 0010b: MTCLKA 0101b: TMCI2 1010b: RXD8/SMISO8/SSCL8 1101b: MOSIA	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI2 01010b: RXD008/SMISO008/ SSCL008 01101b: MOSIA 10001b: USB0_EXICEN 10100b: GTIOC6B 10110b: GTIOC6B# 11000b: GTETRGA 11001b: TS14
PC7PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTCLKB 0101b: TMO2 0111b: CACREF 1010b: TXD8/SMOSI8/SSDA8 1101b: MISOA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTCPPO0 00101b: TMO2 00111b: CACREF 01010b: TXD008/TXDA008/ SMOSI008/SSDA008 01101b: MISOA 10100b: GTIOC6A 10110b: GTIOC6A# 11000b: GTETRGB 11001b: TS13 11011b: LPTO

Table 2.51 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PD0PFS	PSEL[4:0]	—	Pin function select bits
PD1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B	Pin function select bits 00000b: Hi-Z 01011b: RXD6/SMISO6/SSCL6 10000b: CTX0 10100b: GTIOC2A 10110b: GTIOC2A#
PD2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D	Pin function select bits 00000b: Hi-Z 01011b: SCK6 10000b: CRX0 10100b: GTIOC2B 10110b: GTIOC2B#
PD3PFS	PSEL[3:0]	Pin function select bits	—
PD4PFS	PSEL[3:0]	Pin function select bits	—

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PD5PFS	PSEL[3:0]	Pin function select bits	—
PD6PFS	PSEL[3:0]	Pin function select bits	—
PD7PFS	PSEL[3:0]	Pin function select bits	—
PDnPFS	ASEL	—	Analog function select bit

Table 2.52 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PE1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4C 1100b: TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOVLO 01100b: TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12 10100b: GTIOC1B 10110b: GTIOC1B#
PE2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4A 1100b: RXD12/RXDX12/ SMISO12/SSCL12	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOVUP 01100b: RXD12/RXDX12/ SMISO12/SSCL12 10100b: GTIOC1A 10110b: GTIOC1A# 11001b: TS35
PE3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4B 0111b: POE8# 1100b: CTS12#/RTS12#/SS12#	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWUP 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 10100b: GTIOC2A 10101b: GTIOC4B 10110b: GTIOC2A# 10111b: GTIOC4B# 11001b: TS34

Register	Bit	RX210 (n = 0 to 7)	RX261 (n = 0 to 7)
PE4PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4D 0010b: MTIOC1A	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC4A# 00010b: GTOVUP 00011b: GTOWLO 01001b: CLKOUT 10100b: GTIOC1A 10101b: GTIOC2B 10110b: GTIOC1A# 10111b: GTIOC2B# 11000b: GTIOC4A 11001b: TS33
PE5PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC4C 0010b: MTIOC2B	Pin function select bits b4 b0 00000b: Hi-Z 10000b: CMPOB0 10100b: GTIOC1B 10101b: GTIOC5B 10110b: GTIOC1B# 10111b: GTIOC5B#
PE5PFS	PSEL[3:0]	Pin function select bits	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (145/144/100/80/69/64/48-pin) PE5: IRQ5 (145/144/100/80/69/64-pin) PE6: IRQ6 (145/144/100-pin) PE7: IRQ7 (145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (100/80/64/48-pin) PE5: IRQ5 (100/80/64-pin) PE6: IRQ6 (100-pin) PE7: IRQ7 (100-pin)
PEnPFS	ASEL	Analog function select bit 0: Used as other than an analog pin. 1: Used as an analog pin. PE0: AN008 (145/144/100/80/69/64-pin) PE1: AN009 or CMPB0 (145/144/100/80/69/64/48-pin) PE2: AN010 or CVREFB0 (145/144/100/80/69/64/48-pin) PE3: AN011 or CMPA1 (145/144/100/80/69/64/48-pin) PE4: AN012 or CMPA2 (145/144/100/80/69/64/48-pin) PE5: AN013 (145/144/100/80/69/64-pin) PE6: AN014 (145/144/100-pin) PE7: AN015 (145/144/100-pin)	Analog function select bit 0: Used as other than an analog pin. 1: Used as an analog pin. PE0: AN016 (100/80/64-pin) PE1: AN017 or CMPB0 (100/80/64/48-pin) PE2: AN018 or CVREFB0 (100/80/64/48-pin) PE3: AN019 (100/80/64/48-pin) PE4: AN020 or CMPA2 (100/80/64/48-pin) PE5: AN021 (100/80/64-pin) PE6: AN022 (100-pin) PE7: AN023 (100-pin)

Table 2.53 Comparison of PF5 Pin Function Control Register (PF5PFS)

Register	Bit	RX210	RX261
PF5PFS	—	PF5 pin function control register	—

Table 2.54 Comparison of PHn Pin Function Control Registers (PHnPFS)

Register	Bit	RX210 (n = 0 to 3)	RX261 (n = 0 to 3)
PH0PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0111b: CACREF	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOUUP 00111b: CACREF 10100b: GTIOC0A 10110b: GTIOC0A# 11001b: TS10
PH1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0101b: TMO0	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOULO 00101b: TMO0 10100b: GTIOC0B 10110b: GTIOC0B# 11001b: TS9
PH2PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0101b: TMRI0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 10100b: GTIOC1B 10110b: GTIOC1B# 11001b: TS8
PH3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0101b: TMCI0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 10100b: GTIOC2B 10110b: GTIOC2B# 11001b: TS7

Table 2.55 Comparison of PJn Pin Function Control Registers (PJnPFS)

Register	Bit	RX210 (n = 1, 3)	RX261 (n = 1, 3, 6, 7)
PJ1PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3A	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTCPPO0 10100b: GTIOC6A 10110b: GTIOC6A#

Register	Bit	RX210 (n = 1, 3)	RX261 (n = 1, 3, 6, 7)
PJ3PFS	PSEL[3:0] (RX210) PSEL[4:0] (RX261)	Pin function select bits b3 b0 0000b: Hi-Z 0001b: MTIOC3C 1010b: CTS0#/RTS0#/SS0# 1011b: CTS6#/RTS6#SS6#	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 10100b: GTIOC6B 10110b: GTIOC6B#
PJnPFS	ASEL	—	Analog function select bit

Table 2.56 Comparison of PKn Pin Function Control Register (PKnPFS)

Register	Bit	RX210 (n = 2 to 5)	RX261
PKnPFS	—	PKn pin function control register	—

Table 2.57 Comparison of Multi-Function Pin Controller Registers

Register	Bit	RX210	RX261
PFCSE	—	CS output enable register	—
PFAOE0	—	Address output enable register 0	—
PFAOE1	—	Address output enable register 1	—
PFBCR0	—	External bus control register 0	—
PFBCR1	—	External bus control register 1	—

2.18 8-Bit Timer

Table 2.58 shows a Comparative Overview of 8-Bit Timers.

Table 2.58 Comparative Overview of 8-Bit Timers

Item	RX210 (TMR)	RX261 (TMRa)
Count clock	• Frequency dividing clocks: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock	• Internal clocks: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable from compare match A, compare match B, and external reset signal	Selectable from compare match A, compare match B, and external counter reset signal
Timer output	Output pulses with an arbitrary duty cycle or PWM output	Output pulses with an arbitrary duty cycle or PWM output
Two channel cascading connection	• 16-Bit counter mode 16-bit timer using TMR0 as the upper 8 bits and TMR1 as the lower 8 bits (or TMR2 as the upper 8 bits and TMR3 as the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (and TMR3 can be used to count TMR2 compare matches).	• 16-Bit counter mode 16-bit timer using TMR0 as the upper 8 bits and TMR1 as the lower 8 bits (or TMR2 as the upper 8 bits and TMR3 as the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (and TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0, TMR2)	Compare match A, compare match B, and overflow (TMR0, TMR2)
Event link function (input)	(1) Count start operation (TMR0, TMR2) (2) Event counter operation (TMR0, TMR2) (3) Count restart operation (TMR0, TMR2)	Event reception can trigger one of the following three operations: (1) Count start operation (TMR0, TMR2) (2) Event counter operation (TMR0, TMR2) (3) Count restart operation (TMR0, TMR2)
DTC activation	DTC can be activated by compare match A interrupts or compare match B interrupts.	DTC can be activated by compare match A interrupts or compare match B interrupts.
SCI baud rate clock generation (RX210) SCI base clock generation (RX261)	Generates the SCI baud rate clock	Generates the SCI base clock
REMC receive clock generation	—	Generates the operating clock for REMC (remote control signal receiver)
Low power consumption function	Can transition to module stop state at the unit level	Can transition to module stop state at the unit level

2.19 Realtime Clock

Table 2.59 shows a Comparative Overview of Realtime Clocks and Table 2.60 shows a Comparison of Realtime Clock Registers.

Table 2.59 Comparative Overview of Realtime Clocks

Item	RX210 (RTCb)	RX261 (RTCBa)
Count mode	—	Calendar count mode/ binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (crystal resonator or external clock) or main clock (EXTAL)
Clock and calendar functions	• Year, month, date, day-of-week, hour, minute, and second are counted and represented in BCD • 12 hour/24 hour mode switching function • 30-second adjustment function (times less than 30 seconds are rounded down to 00 seconds, and times of 30 seconds or higher are rounded up to one minute) • Automatic adjustment function for leap years • Start/stop function • State of 1, 2, 4, 8, 16, 32, or 64-Hz is represented in binary • Clock error correction function • Output a 1-Hz clock	• Binary count mode Seconds are counted in 32 bits and represented in binary • Calendar count mode — Year, month, date, day-of-week, hour, minute, and second are counted and represented in BCD — 12 hour/24 hour mode switching function — 30-second adjustment function (times less than 30 seconds are rounded down to 00 seconds, and times of 30 seconds or higher are rounded up to one minute) — Automatic adjustment function for leap years • Common to both modes — Start/stop function — Sub-second digits are represented in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output

Item	RX210 (RTCb)	RX261 (RTCBa)
Interrupts	• Alarm interrupt (ALM) Year, month, date, day-of-week, hour, minute, or second can be selected as the alarm interrupt condition.	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected — Binary count mode: Each bit of the 32-bit binary counter
	• Periodic interrupt (PRD) Select an interrupt period of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second.	• Periodic interrupt (PRD) Select an interrupt period of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second.
	• Carry interrupt (CUP) Indicates occurrence of a carry to the seconds counter or a carry to the 64-Hz counter during reading of the 64-Hz counter	• Carry interrupt (CUP) An interrupt is generated at either of the following timing: — When a carry is generated from the 64-Hz counter to the second counter — When a change in the 64-Hz counter coincides with reading from the R64CNT register
	• Recovery from software standby mode or deep software standby mode can be triggered by an alarm interrupt or periodic interrupt.	• Recovery from software standby mode can be triggered by an alarm interrupt or periodic interrupt
Time capture function	• Time capture is implemented by input of three events. At each input event, the system captures the month, day, hour, minute, and second.	• Time capture is implemented by edge detection of the time capture event input pin. At each input event, the system captures the month, day, hour, minute, and second, or a 32-bit binary counter value.
Event link function	Periodic event output	Periodic event output

Table 2.60 Comparison of Realtime Clock Registers

Register	Bit	RX210 (RTCb)	RX261 (RTCBa)
BCNT0	—	—	Binary counter 0
BCNT1	—	—	Binary counter 1
BCNT2	—	—	Binary counter 2
BCNT3	—	—	Binary counter 3
BCNT0AR	—	—	Binary counter 0 alarm register
BCNT1AR	—	—	Binary counter 1 alarm register
BCNT2AR	—	—	Binary counter 2 alarm register
BCNT3AR	—	—	Binary counter 3 alarm register
BCNT0AER	—	—	Binary counter 0 alarm enable register
BCNT1AER	—	—	Binary counter 1 alarm enable register
BCNT2AER	—	—	Binary counter 2 alarm enable register
BCNT3AER	—	—	Binary counter 3 alarm enable register
RCR1	RTCOS	—	RTCOUT output select bit
RCR2	AADJP	Automatic adjustment period select bit 0: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every one minute. 1: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every ten seconds.	Automatic adjustment period select bit 0: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every one minute (or every 32 seconds in binary counter mode). 1: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every ten seconds (or every 8 seconds in binary counter mode).
	CNTMD	—	Count mode select bit
RCR3	—	RTC control register 3	—
BCNT0CPn	—	—	BCNT0 capture register n (n = 0 to 2)
BCNT1CPn	—	—	BCNT1 capture register n (n = 0 to 2)
BCNT2CPn	—	—	BCNT2 capture register n (n = 0 to 2)
BCNT3CPn	—	—	BCNT3 capture register n (n = 0 to 2)

2.20 Watchdog Timer

Table 2.61 shows a Comparative Overview of Watchdog Timers.

Table 2.61 Comparative Overview of Watchdog Timers

Item	RX210 (WDTA)	RX261 (WDTA)
Count source	Peripheral clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	Divided by 4, 64, 128, 512, 2048, or 8192	Divided by 4, 64, 128, 512, 2048, or 8192
Count operation	Count down using 14-bit down-counter	Count down using 14-bit down-counter
Count start conditions	• Auto start mode: Counting starts automatically after a reset is released • Register start mode: Counting starts when triggered by a refresh operation (writing 00h and then FFh to the WDTRR register)	• Auto start mode: Counting starts automatically after a reset is released • Register start mode: Counting starts when triggered by a refresh operation (writing 00h and then FFh to the WDTRR register)
Count stop conditions	• Reset (the down-counter and other registers return to their initial values) • An underflow or refresh error occurs • Counting restarts — Auto-start mode: Counting restarts automatically after a reset or non-maskable interrupt request is output. — Register start mode: Counting restarts after refreshing the counter	• Reset • Entering low power consumption mode • An underflow or refresh error occurs (in register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources (RX210) Watchdog timer reset sources (RX261)	• Down-counter underflows • A refresh occurs outside a refresh-permitted period (refresh error)	• Down-counter underflows • A refresh occurs outside a refresh-permitted period (refresh error)
Interrupt request output sources (RX210) Non-maskable interrupt sources (RX261)	• A non-maskable interrupt (WUNI) is generated when the down-counter underflows • A refresh occurs outside a refresh-permitted period (refresh error)	• Down-counter underflows • A refresh occurs outside a refresh-permitted period (refresh error)
Reading counter value	• The value of the down-counter can be read by reading the WDTSR register.	• The value of the down-counter can be read by reading the WDTSR register.
Output signal (internal signal)	• Reset output • Interrupt request output	• Reset output • Interrupt request output

Item	RX210 (WDTA)	RX261 (WDTA)
Auto start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock division ratio after a reset (OFS0.WDTCKS[3:0] bits) Selecting the timeout period of the watchdog timer (OFS0.WDTTOPS[1:0] bits) Selecting the window start position of the watchdog timer (OFS0.WDTRPSS[1:0] bits) Selecting the window end position of the watchdog timer (OFS0.WDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.WDTRSTIRQS bit)	• Selecting the clock division ratio after a reset (OFS0.WDTCKS[3:0] bits) Selecting the timeout period of the watchdog timer (OFS0.WDTTOPS[1:0] bits) Selecting the window start position of the watchdog timer (OFS0.WDTRPSS[1:0] bits) Selecting the window end position of the watchdog timer (OFS0.WDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.WDTRSTIRQS bit)
Register start mode (WDT register control)	• Selecting the clock division ratio after a refresh operation (WDTCR.CKS[3:0] bits) • Selecting the timeout period of the watchdog timer (WDTCR.TOPS[1:0] bits) Selecting the window start position of the watchdog timer (WDTCR.RPSS[1:0] bits) Selecting the window end position of the watchdog timer (WDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (WDTRCR.RSTIRQS bit)	• Selecting the clock division ratio after a refresh operation (WDTCR.CKS[3:0] bits) • Selecting the timeout period of the watchdog timer (WDTCR.TOPS[1:0] bits) Selecting the window start position of the watchdog timer (WDTCR.RPSS[1:0] bits) Selecting the window end position of the watchdog timer (WDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (WDTRCR.RSTIRQS bit)

2.21 Independent Watchdog Timer (IWDT)

Table 2.62 shows a Comparative Overview of Independent Watchdog Timers and Table 2.63 shows a Comparison of Independent Watchdog Timer Registers.

Table 2.62 Comparative Overview of Independent Watchdog Timers

Item	RX210 (IWDTa)	RX261 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Divided by 1, 16, 32, 64, 128, or 256	Divided by 1, 16, 32, 64, 128, or 256
Count operation	Count down using 14-bit down-counter	Count down using 14-bit down-counter
Count start conditions	• Auto start mode: Counting starts automatically after a reset • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register)	• Auto-start mode: Counting starts automatically after a reset is released • Register start mode: Counting starts when triggered by a refresh operation (writing 00h and then FFh to the IWDTRR register)
Count stop conditions	• Reset (the down-counter and other registers return to their initial values) • An underflow or refresh error occurs • Counting restarts — Auto-start mode: Counting restarts automatically after a reset or non-maskable interrupt request is output. — Register start mode: Counting restarts after refreshing the counter	• Reset • Entering low power consumption mode (depends on register setting) • An underflow or refresh error occurs (in register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • A refresh occurs outside a refresh-permitted period (refresh error)	• Down-counter underflows • A refresh occurs outside a refresh-permitted period (refresh error)
Interrupt request output sources (RX210) Non-maskable interrupt sources (RX261)	• A non-maskable interrupt (WUNI) is generated when the down-counter underflows. • A refresh occurs outside a refresh-permitted period (refresh error)	• Down-counter underflows • A refresh occurs outside a refresh-permitted period (refresh error)
Reading counter value	• The value of the down-counter can be read by reading the IWDTSR register.	• The value of the down-counter can be read by reading the IWDTSR register.
Event link function (output)	• Down-counter underflows • A refresh occurs outside a refresh-permitted period (refresh error)	• Down-counter underflow event output • Refresh error event output

Item	RX210 (IWDTa)	RX261 (IWDTa)
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output
Auto start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (IWDT register control)	• Selecting the clock division ratio after a refresh operation (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock division ratio after a refresh operation (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position of the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position of the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Table 2.63 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX210 (IWDTa)	RX261 (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting is stopped at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting is stopped at transition to sleep mode, software standby mode, or deep sleep mode

2.22 Serial Communications Interface

Table 2.64 shows a Comparative Overview of Serial Communication Interfaces, Table 2.65 shows a Comparison of SCI Channel Specifications, and Table 2.66 shows a Comparison of Serial Communication Interface Registers.

Table 2.64 Comparative Overview of Serial Communication Interfaces

Item		RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
Number of channels		• SCIc: 12 channels • SCId: 1 channel	• SCIk: 3 channels • SCIh: 1 channel
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator	Bit rate specifiable by on-chip baud rate generator
Full-duplex communications		• Transmitter: Continuous transmission is enabled by a double-buffer configuration • Receiver: Continuous reception is enabled by a double-buffer configuration	• Transmitter: Continuous transmission is enabled by a double-buffer configuration • Receiver: Continuous reception is enabled by a double-buffer configuration
Data transfer		Selectable between LSB first and MSB first	Selectable between LSB first and MSB first
I/O signal level inversion		—	The levels of input and output signals can be inverted independently (SCI1, SCI5, and SCI6)
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completed generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, and receive error (all channels), and data match (SCI1, SCI5, and SCI6) • Completed generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Individual channels can transition to module stop state	Individual channels can transition to module stop state
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity function	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity error, overrun error, or framing error	Parity error, overrun error, or framing error
	Hardware flow control	CTSn and RTSn pins can be used to control transmission and reception.	CTSn# and RTSn# pins can be used to control transmission and reception.

Item		RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
Asynchronous mode	Data match detection	—	Compares receive data with the contents of a comparison data register and generates an interrupt request when they match. (SCI1, SCI5, and SCI6)
	Start-bit detection	—	Selection of low level or falling edge
	Adjustment of receive data sampling timing	—	The sampling point of the receive data can be shifted forward or backward relative to the center of the data. (SCI1, SCI5, and SCI6)
	Adjustment of transmit signal transition timing	—	The falling or rising edge of the transmit data can be delayed. (SCI1, SCI5, and SCI6)
	Break detection	When a framing error occurs, breaks can be detected by reading the RXDn pin level directly.	When a framing error occurs, breaks can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag (SCI1, SCI5, and SCI6).
	Clock source	• An internal or external clock can be selected. • The transfer rate clock can be input from the TMR. (SCI5, SCI6, and SCI12)	• An internal or external clock can be selected. • The transfer rate clock can be input from the TMR. (SCI5, SCI6, and SCI12)
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Function for serial communication among multiple processors	Function for serial communication among multiple processors
	Noise cancellation	Digital noise filters are built into the signal paths from input on the RXDn pins	Digital noise filters are built into the signal paths from input on the RXDn pins.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn and RTSn pins can be used to control transmission and reception.	CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when a parity error is detected during reception. • Data can be automatically re-sent when an error signal is received during transmission	• An error signal can be automatically transmitted when a parity error is detected during reception. • Data can be automatically re-sent when an error signal is received during transmission
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention
Simple I^2C mode	Communication format	I^2C bus format (MSB-first transfer only)	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Up to 384 kbps	Support for fast mode

Item		RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
Simple I²C mode	Noise cancellation	• Digital noise filters are built into the SSCLn and SSDAn input signal paths • Adjustable noise cancellation width	• Digital noise filters are built into the SSCLn and SSDAn input signal paths • Adjustable noise cancellation width
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state
	Clock settings	There are four options for clock phase and clock polarity settings	There are four options for clock phase and clock polarity settings
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Support for break field low width output and generation of interrupt on output completion • Support for detection of bus collision and generation of interrupt on detection	• Support for break field low width output and generation of interrupt on output completion • Support for detection of bus collision and generation of interrupt on detection
	Start frame reception	• Support for break field low width detection and generation of interrupt on detect completion • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two types of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rate	• Support for break field low width detection and generation of interrupt on detect completion • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two types of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rate
	I/O control function	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signals • Half-duplex communication employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select timing of receive data sampling for RXDX12 pin • Signals received on RXDX12 can be passed through to SCIc when the extended serial mode control section is off.	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signals • Half-duplex communication employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select timing of receive data sampling for RXDX12 pin
	Timer function	Usable as reload timer	Usable as reload timer

Item	RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
Bit rate modulation function	—	Errors can be reduced by correcting the output of the on-chip baud rate generator
Event link function (supported by SCI5 only)	• Error event output (receive error or error signal detection) • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error event output (receive error or error signal detection) • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.65 Comparison of SCI Channel Specifications

Item	RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
Asynchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Simple I^2C mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI1, SCI5, SCI6, SCI12
Data match detection	—	SCI1, SCI5, SCI6
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5

Table 2.66 Comparison of Serial Communication Interface Registers

Register	Bit	RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
RDRH, RDRL, RDRHL	—	—	Receive data register H, L, HL
TDRH, TDRL, TDRHL	—	—	Transmit data register H, L, HL
SMR	CHR	Character length bit (Valid only in asynchronous mode) 0: Uses 8 bits as the data length for transmission and reception 1: Uses 7 bits as the data length for transmission and reception	Character length bit (Valid only in asynchronous mode) Selected in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Uses 9 bits as the data length for transmission and reception 0 1: Uses 9 bits as the data length for transmission and reception 1 0: Uses 8 bits as the data length for transmission and reception (initial value) 1 1: Uses 7 bits as the data length for transmission and reception
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode	Communications mode bit 0: Asynchronous mode or simple I^2C mode 1: Clock synchronous mode or simple SPI mode

Register	Bit	RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
SCR	CKE[1:0]	Clock enable bits In serial communications interface mode (SCMR.SMIF bit = 0) (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin can be used as an I/O port according to the I/O port settings. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. • For SCI to SCI4 and SCI7 to SCI11 b1 b0 1 x: External clock A clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1. • For SCI5, SCI6, and SCI12 b1 b0 1 x: External clock or TMR clock — When an external clock is used, a clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1. — The TMR clock can be used. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	Clock enable bits In non-smart card interface mode (SCMR.SMIF bit = 0) (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin becomes high-impedance. 0 1: On-chip baud rate generator The clock with the same frequency as the bit rate is output from the SCKn pin. • For SCI5, SCI6, and SCI12 b1 b0 1 x: External clock or TMR clock — When an external clock is used, a clock with a frequency 16 times the bit rate should be input from the SCKn pin. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is set to 1. — The SCKn pin becomes high-impedance when the TMR clock is used. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.

Register	Bit	RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
SCR	CKE[1:0]	In smart card interface mode (SCMR.SMIF=1) • When the SMR.GM bit = 0 b1 b0 0 0: Output disabled (The SCKn pin can be used as an I/O port according to the I/O port settings.) 0 1: Clock output 1 x: (Setting prohibited) • When the SMR.GM bit = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high	In smart card interface mode (SCMR.SMIF=1) • When the SMR.GM bit = 0 b1 b0 0 0: Output disabled The SCKn pin becomes high-impedance. 0 1: Clock output 1 x: Setting prohibited • When the SMR.GM bit = 1 b1 b0 0 0: Output fixed low x 1: Clock output 1 0: Output fixed high
SSR	RDRF	—	Receive data full flag
	TDRE	—	Transmit data empty flag
SCMR	SMIF	Smart card interface mode select bit 0: Serial communications interface mode 1: Smart card interface mode	Smart card interface mode select bit 0: Non-smart card interface mode (Asynchronous mode, clock synchronous mode, simple SPI mode, or simple I²C mode) 1: Smart card interface mode
	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register
SEMR	ITE	—	Instant transmission enable bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
SPMR	MSS	Master slave select bit 0: Transmission is through the TXDn pin and reception is through the RXDn pin (master mode). 1: Reception is through the TXDn pin and transmission is through the RXDn pin (slave mode).	Master slave select bit 0: Transmission is through the SMOSIn pin and reception is through the SMISOn pin (master mode). 1: Reception is through the SMOSIn pin and transmission is through the SMISOn pin (slave mode).
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register

Register	Bit	RX210 (SCIc, SCId)	RX261 (SCIk, SCIh)
CR2	BCCS[1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited	Bus collision detection clock select bits • When the SEMR.BGDM bit is set to 0, or the SEMR.BGDM bit is set to 1 and the SMR.CKS[1:0] bits are set to a value other than 00b b5 b4 0 0: Base clock 0 1: Base clock frequency divided by 2 1 0: Base clock frequency divided by 4 1 1: Setting prohibited • When the SEMR.BGDM bit is set to 1 and the SMR.CKS[1:0] bits are set to 00b b5 b4 0 0: Base clock frequency divided by 2 0 1: Base clock frequency divided by 4 1 0: Setting prohibited 1 1: Setting prohibited

2.23 I²C Bus Interface

Table 2.67 shows a Comparison of I²C Bus Interface Registers.

Table 2.67 Comparison of I²C Bus Interface Registers

Register	Bit	RX210 (RIIC)	RX261 (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNT	—	Timeout internal counter	—

2.24 Serial Peripheral Interface

Table 2.68 shows a Comparative Overview of Serial Peripheral Interfaces and Table 2.69 shows a Comparison of Serial Peripheral Interface Registers.

Table 2.68 Comparative Overview of Serial Peripheral Interfaces

Item	RX210 (RSPI)	RX261 (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is possible. • The polarity of the serial transfer clock can be changed. • The phase of the serial transfer clock can be changed.	• Use of MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or simplex (transmit-only) can be selected • The RSPCK polarity can be changed. • The RSPCK phase can be changed
Data format	• Selectable between MSB first and LSB first • Transfer bit length is selectable from 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transfer/receive buffers • A maximum of four frames can be transferred in one instance of transmission/reception (with each frame consisting of a maximum of 32 bits).	• Selectable between MSB first and LSB first • Transfer bit length is selectable from 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transfer/receive buffers • A maximum of four frames can be transferred in one instance of transmission/reception (with each frame consisting of a maximum of 32 bits). • Transmit and receive data can be swapped in byte units
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the maximum divisor is 4096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is the PCLK frequency divided by 8). — Width at high level: Four PCLK cycles — Width at low level: Four PCLK cycles	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is PCLK frequency divided by 4). — Width at high level: Two PCLK cycles — Width at low level: Two PCLK cycles
Buffer configuration	• Double buffer configuration for transmit and receive buffers	• Double buffer configuration for transmit and receive buffers • 128-bit transmit and receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX210 (RSPI)	RX261 (RSPIc)
SSL control function	• Four SSL signals per channel (SSLA0 to SSLA3) • In single-master mode, SSLA0 to SSLA3 are output pins. • In multi-master mode, SSLA0 is an input pin, and SSLA1 to SSLA3 are either output pins or unused. • In slave mode, SSLA0 is an input pin, and SSLA1 to SSLA3 are unused. • Configurable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Configurable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Configurable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins per channel (SSLA0 to SSLA3) • In single-master mode, SSLA0 to SSLA3 are output pins. • In multi-master mode, SSLA0 is an input pin, and SSLA1 to SSLA3 are either output pins or unused. • In slave mode, SSLA0 is an input pin, and SSLA1 to SSLA3 are unused. • Configurable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Configurable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Configurable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer mode	• Transfers of a maximum of eight commands can be executed sequentially in a loop. • The following can be set for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value are configurable on SSL negation	Transfers of a maximum of eight commands can be executed sequentially in a loop • The following can be set for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value are configurable on SSL negation • RSPCK auto-stop function
Interrupt sources	• Maskable interrupt sources — RSPI receive interrupt (receive buffer full) — RSPI transmit interrupt (transmit buffer empty) — RSPI error interrupt (mode fault, overrun, or parity error) — RSPI idle interrupt (RSPI idle)	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt

Item	RX210 (RSPIc)	RX261 (RSPIc)
Event link function (output)	• The following five types of events can be output to the event link controller: — Receive-buffer full event output — Transmit-buffer empty event output — Mode fault, overrun, or parity error event output — RSPI idle event output — Transmit end event output	• The following events can be output to the event link controller (RSPI0): — Receive buffer full event — Transmit buffer empty event — Error event (mode fault, overrun, underrun, or parity error) — Idle event — Transmit end event
Others	• CMOS/open drain output switching function • RSPI initialization function • Loopback mode	• RSPI initialization function • Loopback mode
Low power consumption function	Ability to enable module stop state	Ability to enable module stop state

Table 2.69 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX210 (RSPI)	RX261 (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error 1: Mode fault error	Mode fault error flag 0: No mode fault error, no underrun error 1: Mode fault error or underrun error
	UDRF	—	Underrun error flag
	SPTEF	—	Transmit buffer empty flag
	SPRF	—	Receive buffer full flag
SPDR	—	RSPI data register Accessible size • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Accessible size • Longword access (SPDCR.SPLW = 1, SPBYTE = 0) • Word access (SPDCR.SPLW = 0, SPBYTE = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: A parity bit is not added to transmit data and no parity check of receive data is performed 1: A parity bit is added to transmit data and a parity check of receive data is performed (when SPCR.TXMD = 0) A parity bit is added to transmit data but no parity check of receive data is performed (when SPCR.TXMD = 1)	Parity enable bit 0: A parity bit is not added to transmit data and no parity check of receive data is performed 1: A parity bit is added to transmit data and a parity check of receive data is performed
	SCKASE	—	RSPCK auto-stop function enable bit
SPDCR2	—	—	RSPI data control register 2

2.25 12-Bit A/D Converter

Table 2.70 shows a Comparative Overview of 12-Bit A/D Converters and Table 2.71 shows a Comparison of 12-Bit A/D Converter Registers.

Table 2.70 Comparative Overview of 12-Bit A/D Converters

Item	RX210 (S12ADb)	RX261 (S12ADE)
Number of units	1 unit	1 unit
Input channels	16 channels	25 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	Per channel: 1.0 µs (when A/D conversion clock ADCLK = 50 MHz)	Per channel: 0.7 µs (ADCCR.CCS bit = 0), 0.5 µs (ADCCR.CCS bit = 1) (when A/D conversion clock ADCLK = 64 MHz)
A/D conversion clock	The peripheral module clock PCLK and A/D conversion clock ADCLK can be set to the following frequency ratios: — PCLK to ADCLK frequency ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1 ADCLK is set using the clock generation circuit.	The peripheral module clock PCLKB and A/D conversion clock ADCLK can be set to the following frequency ratios: — PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data registers	• 16 registers for analog input • One register for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • The results of A/D conversion are stored in 12-bit A/D data registers • In addition mode, A/D conversion results are added and stored in A/D data registers as 14-bit data. • Duplication of A/D-converted data — The first instance of A/D conversion data for analog input of a selected channel is stored in A/D data register y, and the second instance is stored in the duplication register. — Duplication is only available when double trigger mode is selected in single scan mode or group scan mode.	• 25 registers for analog input • One register for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • Support for A/D conversion results to be output with 12-bit accuracy • In addition mode, A/D conversion results are added and stored in A/D data registers as data whose number of bits is the number of bits for conversion accuracy + 2 bits/4 bits. • Double trigger mode (available in single scan mode or group scan mode) — The first instance of A/D conversion data for analog input of a selected channel is stored in the data register for the channel, and the second instance is stored in the duplication register.

Item	RX210 (S12ADb)	RX261 (S12ADE)
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of a maximum of 16 arbitrarily selected channels. — A/D conversion is performed only once on the temperature sensor output — A/D conversion is performed only once on the internal reference voltage • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of a maximum of 16 arbitrarily selected channels. • Group scan mode: — The analog inputs of a maximum of 16 channels are divided into group A and group B, and A/D conversion of the analog inputs selected at the group level is performed only once for all channels — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of a maximum of 25 arbitrarily selected channels — A/D conversion is performed only once on the temperature sensor output — A/D conversion is performed only once on the internal reference voltage • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of a maximum of 25 arbitrarily selected channels • Group scan mode: — The analog inputs of a maximum of 25 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected at the group level is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode: (when group A priority control is selected) — If a trigger for group A is input during A/D conversion of group B, A/D conversion of group B is stopped and A/D conversion is performed for group A. — A/D conversion can be configured to restart (rescan) for group B after A/D conversion of group A has completed.
A/D conversion start conditions	• Software trigger • Synchronous trigger Trigger from MTU, ELC, or temperature sensor • Asynchronous trigger A/D conversion can be initiated by the external trigger ADTRG0# pin	• Software trigger • Synchronous trigger Trigger from the general-purpose PWM timer (GPTW) or event link controller (ELC) • Asynchronous trigger A/D conversion can be initiated by the external trigger ADTRG0# pin

Item	RX210 (S12ADb)	RX261 (S12ADE)
Functions	• Sample-and-hold function • Channel-dedicated sample-and-hold function (0.25 V ≤ analog voltage input ≤ AVCC0 - 0.25 V) • Variable sampling state count function • Self-diagnosis function of 12-bit A/D converter • A/D-converted value addition mode • Analog input disconnection detection assist function • Double trigger mode (A/D-converted data duplication function)	• Variable sampling state count function • Self-diagnosis function of 12-bit A/D converter • Option to select between A/D-converted value addition mode and average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (A/D-converted data duplication function) • A/D data register automatic clear function • Compare function (window A and window B) • 16 ring buffers when using the compare function
Interrupt sources	• Except in double trigger mode and group scan mode, scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, the scan end interrupt request (S12ADI0) is generated on completion of a double scan. • In group scan mode, the scan end interrupt request (S12ADI0) is generated when scanning of group A has completed. A scan end interrupt request (GBADI) exclusive to group B is generated when scanning of group B has completed. • When double trigger mode is selected in group scan mode, the scan end interrupt request (S12ADI0) is generated at the completion of a double scan for group A. A scan end interrupt request (GBADI) exclusive to group B is generated when scanning of group B has completed. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).	• Except in double trigger mode and group scan mode, scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, the scan end interrupt request (S12ADI0) is generated on completion of a double scan. • In group scan mode, the scan end interrupt request (S12ADI0) is generated when scanning of group A has completed. A scan end interrupt request (GBADI) exclusive to group B is generated when scanning of group B has completed. • When double trigger mode is selected in group scan mode, the scan end interrupt request (S12ADI0) is generated at the completion of a double scan for group A. A scan end interrupt request (GBADI) exclusive to group B is generated when scanning of group B has completed. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).
Event link function	• An ELC event is generated on scan completion except when the completed scan is of group B in group scan mode. • Scanning can be initiated by a trigger from the ELC.	• An ELC event is generated on scan completion except when the completed scan is of group B in group scan mode. • An ELC event is generated on completion of a scan of group B in group scan mode. • An ELC event is generated on completion of all scans. • Scanning can be initiated by a trigger from the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode

Item	RX210 (S12ADb)	RX261 (S12ADE)
Low power consumption function	Ability to enable module stop state	Ability to enable module stop state

Table 2.71 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX210 (S12ADb)	RX261 (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 15) The format differs depending on the following conditions. • Settings of the A/D data register format select bit (ADCER.ADRFMT) (right-justified or left-justified) • Selection of A/D-converted value addition mode	A/D data register y (y = 0 to 8,16 to 31) The format differs depending on the following conditions. • Settings of the A/D data register format select bit (ADCER.ADRFMT) (right-justified or left-justified) • Settings of the addition count select bits (ADADC.ADC[2:0]) • Settings of the average mode enable bit (ADADC.AVEE) (add or average)
ADDBLDR	—	A/D data duplication register The format differs depending on the following conditions. • Settings of the A/D data register format select bit (ADCER.ADRFMT) (right-justified or left-justified) • Selection of A/D-converted value addition mode	A/D data duplication register The format differs depending on the following conditions. • Settings of the A/D data register format select bit (ADCER.ADRFMT) (right-justified or left-justified) • Settings of the addition count select bits (ADADC.ADC[2:0]) • Settings of the average mode enable bit (ADADC.AVEE) (add or average)
ADTSDR	—	A/D temperature sensor data register The format differs depending on the following conditions. • Settings of the A/D data register format select bit (ADCER.ADRFMT) (right-justified or left-justified) • Selection of A/D-converted value addition mode	A/D temperature sensor data register The format differs depending on the following conditions. • Settings of the A/D data register format select bit (ADCER.ADRFMT) (right-justified or left-justified) • Settings of the addition count select bits (ADADC.ADC[2:0]) • Settings of the average mode enable bit (ADADC.AVEE) (add or average)

Register	Bit	RX210 (S12ADb)	RX261 (S12ADE)
ADOCDR	—	A/D internal reference voltage data register The format differs depending on the following conditions. • Settings of the A/D data register format select bit (ADCER.ADRFMT) (right-justified or left-justified) • Selection of A/D-converted value addition mode	A/D internal reference voltage data register The format differs depending on the following conditions. • Settings of the A/D data register format select bit (ADCER.ADRFMT) (right-justified or left-justified) • Settings of the addition count select bits (ADADC.ADC[2:0]) • Settings of the average mode enable bit (ADADC.AVEE) (add or average)
ADCSR	ADHSC	—	A/D conversion select bit
ADANSA	—	A/D channel select register A	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	—	—	A/D channel select register A1
ADANSB	—	A/D channel select register B	—
ADANSB0	—	—	A/D channel select register B0
ADANSB1	—	—	A/D channel select register B1
ADADS	—	A/D-converted value addition mode select register	
ADADS0	—	—	A/D-converted value addition/average function channel select register 0
ADADS1	—	—	A/D-converted value addition/average function channel select register 1
ADADC	ADC[1:0] (RX210) ADC[2:0] (RX261)	Addition count select bits b1 b0 0 0: One-time conversion (no addition. Same as normal conversion) 0 1: Two-time conversion (addition once) 1 0: Three-time conversion (addition twice) 1 1: Four-time conversion (addition three times)	Addition count select bits b2 b0 0 0 0: One-time conversion (no addition. Same as normal conversion.) 0 0 1: Two-time conversion (addition once) 0 1 0: Three-time conversion (addition twice) 0 1 1: Four-time conversion (addition three times) 1 0 1: Sixteen-time conversion (addition fifteen times) Settings other than the preceding are prohibited.
	AVEE	—	Average mode enable bit

Register	Bit	RX210 (S12ADb)	RX261 (S12ADE)
ADCER	DIAGVAL[1:0]	Self-diagnosis conversion voltage select bits b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: Uses the voltage of 0 V for self-diagnosis. 1 0: Uses the voltage of VREFH0 × 1/2 for self-diagnosis. 1 1: Uses the voltage of VREFH0 for self-diagnosis.	Self-diagnosis conversion voltage select bits b9 b8 0 0: Setting prohibited in self-diagnosis voltage fixed mode 0 1: Uses the voltage of 0 V for self-diagnosis. 1 0: Uses the voltage of reference voltage × 1/2 for self-diagnosis*1 1 1: Uses the voltage of reference voltage for self-diagnosis*1
ADSTRGR	TRSB[3:0] (RX210) TRSB[5:0] (RX261)	A/D conversion start trigger select bits for group B	A/D conversion start trigger select bits for group B
	TRSA[3:0] (RX210) TRSA[5:0] (RX261)	A/D conversion start trigger select bits	A/D conversion start trigger select bits
ADEXICR	TSSAD	—	Temperature sensor output A/D-converted value addition/average mode select bit
	OCSAD	Internal reference voltage A/D-converted value addition mode select bit 0: Internal reference voltage A/D-converted value addition mode is not selected. 1: Internal reference voltage A/D-converted value addition mode is selected.	Internal reference voltage A/D-converted value addition/average mode select bit 0: Internal reference voltage A/D-converted value addition/average mode is not selected. 1: Internal reference voltage A/D-converted value addition/average mode is selected.
	TSS(RX210) TSSA(RX261)	Temperature sensor output A/D conversion select bit	Temperature sensor output A/D conversion select bit
	OCS(RX210) OCSA(RX261)	Internal reference voltage A/D conversion select bit	Internal reference voltage A/D conversion select bit
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, T, O)	A/D sampling state register n (n = 0 to 8, L, T, O)
	—	The initial value after a reset differs.	
ADSHCR	—	A/D Sample and hold circuit control register	—
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D compare function control register
ADCMPANSR0	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	A/D compare function window A channel select register 1

Register	Bit	RX210 (S12ADb)	RX261 (S12ADE)
ADCMPANSER	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	A/D compare function window A comparison condition setting register 0
ADCMPLR1	—	—	A/D compare function window A comparison condition setting register 1
ADCMPLER	—	—	A/D compare function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D compare function window A lower-side level setting register
ADCMPDR1	—	—	A/D compare function window A upper-side level setting register
ADCMPSR0	—	—	A/D compare function window A channel status register 0
ADCMPSR1	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	A/D compare function window A extended input channel status register
ADHVREFCNT	—	—	A/D high-potential/low-potential reference voltage control register
ADWINMON	—	—	A/D compare function window A/B status monitor register
ADCMPBNSR	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	A/D compare function window B lower-side level setting register
ADWINULB	—	—	A/D compare function window B upper-side level setting register
ADCMPBSR	—	—	A/D compare function window B channel status register
ADBUFn	—	—	A/D data storage buffer register n (n = 0 to 15)
ADBUFEN	—	—	A/D data storage buffer enable register
ADBUFPTR	—	—	A/D data storage buffer pointer register
ADCCR	—	—	A/D conversion cycle control register

Note: 1. The reference voltage means the voltage on the pin selected in the ADHVREFCNT register.

2.26 D/A Converter

Table 2.72 shows a Comparative Overview of D/A Converters and Table 2.73 shows a Comparison of D/A Converter Registers.

Table 2.72 Comparative Overview of D/A Converters

Item	RX210 (DA)	RX261 (DAa)
Resolution	10 bits	8 bits
Output channels	2 channel	2 channel
Measure against mutual interference between analog modules	—	• Measure against interference between D/A conversion and A/D conversion The update timing of D/A converted data is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by using the enable signal to control the timing of the 8-bit D/A converter inrush current.
Low power consumption function	Ability to enable module stop state	Can transition to module stop state
Event link function (input)	Ability to start D/A conversion on channel 0 at event signal input	Ability to start D/A conversion on channel 0 at event signal input

Table 2.73 Comparison of D/A Converter Registers

Register	Bit	RX210 (DA)	RX261 (DAa)
DACR	DAE	D/A enable bit	—
DAADSCR	—	—	D/A A/D synchronous start control register

2.27 Temperature Sensor

Table 2.74 shows a Comparative Overview of Temperature Sensors and Table 2.75 shows a Comparison of Temperature Sensor Registers.

Table 2.74 Comparative Overview of Temperature Sensors

Item	RX210 (TEMPSa)	RX261 (TEMPSA)
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter via a programmable gain amplifier (PGA).	Temperature sensor outputs a voltage to the 12-bit A/D converter.
Low power consumption function	Ability to enable module stop state	—

Table 2.75 Comparison of Temperature Sensor Registers

Register	Bit	RX210 (TEMPSa)	RX261 (TEMPSA)
TSCDR	—	—	Temperature sensor calibration data register
TSCR	—	Temperature sensor control register	—

2.28 Comparator B

Table 2.76 shows a Comparative Overview of Comparator B and Table 2.77 shows a Comparison of Comparator B Registers.

Table 2.76 Comparative Overview of Comparator B

Item	RX210 (CMPB)	RX261 (CMPBa)
Analog input voltage	Input voltage to CMPBn pin	Input voltage to CMPBn pin
Reference input voltage	Input voltage to CVREFBn pin	Input voltage to CVREFBn pin or internal reference voltage
Comparison result	Read from the CPBFLG.CPBnOUT flag	Read from the CPBFLG.CPBnOUT flag The comparison result can be output to the CMPOBn pin.
Interrupt request generation timing	• When the comparison result of comparator B0 changes • When the comparison result of comparator B1 changes	• When the comparison result of comparator B0 changes • When the comparison result of comparator B1 changes
Timing of event generation to ELC	• When the comparison result of comparator B0 changes • When the comparison result of comparator B0 or B1 changes	• When the comparison result of comparator B0 changes • When the comparison result of comparator B0 or B1 changes
POE source output timing	—	• When the comparison result of comparator B0 changes • When the comparison result of comparator B1 changes
Selectable functions	• Digital filter function Select whether to enable the digital filter, and the sampling frequency	• Digital filter function Select whether to enable the digital filter, and the sampling frequency • Window function Select whether the window function (VRFL < CMPBn < VRFH) is enabled or disabled. • Reference input voltage Select between CVREFBn pin input or internal reference voltage (generated internally). • Comparator B response speed Select high-speed mode or low-speed mode
Low power consumption function	Can transition to module stop state	Can transition to module stop state

Table 2.77 Comparison of Comparator B Registers

Register	Bit	RX210 (CMPB)	RX261 (CMPBa)
CPBCNT2	—	—	Comparator B control register 2
CPBFLG	CPB0OUT	Comparator B0 monitor flag 0: CMPB0 < CVREFB0 1: CMPB0 > CVREFB0	Comparator B0 monitor flag When the window function is disabled 0: CMPB0 < CVREFB0 or CMPB0 < internal reference voltage, or comparator B0 operation disabled 1: CMPB0 > CVREFB0 or CMPB0 > internal reference voltage When the window function is enabled 0: CMPB0 < VRFL or CMPB0 > VRFH, or comparator B0 operation disabled 1: VRFL < CMPB0 < VRFH
	CPB1OUT	Comparator B1 monitor flag 0: CMPB1 < CVREFB1 1: CMPB1 > CVREFB1	Comparator B1 monitor flag When the window function is disabled 0: CMPB1 < CVREFB1 or CMPB1 < internal reference voltage, or comparator B1 operation disabled 1: CMPB1 > CVREFB1 or CMPB1 > reference voltage When the window function is enabled 0: CMPB1 < VRFL or CMPB1 > VRFH, or comparator B1 operation disabled 1: VRFL < CMPB1 < VRFH
CPBMD	—	—	Comparator B mode select register
CPBREF	—	—	Comparator B reference input voltage select register
CPBOCR	—	—	Comparator B output control register

2.29 Data Operation Circuit

Table 2.78 shows a Comparative Overview of Data Operation Circuits.

Table 2.78 Comparative Overview of Data Operation Circuits

Item	RX210 (DOC)	RX261 (DOC)
Data operation function	16-bit data comparison, addition, and subtraction	16-bit data comparison, addition, and subtraction
Low power consumption function	Ability to enable module stop state	Can transition to module stop state
Interrupts	—	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh, which is an overflow. • The result of data reduction is less than 0000h, which is an underflow.
Event link function (output)	—	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh, which is an overflow. • The result of data reduction is less than 0000h, which is an underflow.

2.30 RAM

Table 2.79 shows a Comparative Overview of RAM and Table 2.80 shows a Comparison of RAM Registers.

Table 2.79 Comparative Overview of RAM

Item	RX210	RX261
RAM size	Maximum of 96 KB (RAM0: 64 KB, RAM1: 32 KB)	128 KB
RAM addresses	• 96 KB RAM0: 0000 0000h to 0000 FFFFh RAM1: 0001 0000h to 0001 7FFFh • 64 KB RAM0: 0000 0000h to 0000 FFFFh • 32 KB RAM0: 0000 0000h to 0000 7FFFh • 20 KB RAM0: 0000 0000h to 0000 4FFFh • 16 KB RAM0: 0000 0000h to 0000 3FFFh • 12 KB RAM0: 0000 0000h to 0000 2FFFh	• RAM: 0000 0000h to 0001 FFFFh
Memory bus	Memory bus 1	Memory bus 1
Access	• Read and write access are both performed in a single cycle. • RAM can be enabled or disabled.	• Read and write access are both performed in a single cycle.*1 • RAM can be enabled or disabled.
Low power consumption function	The module stop state can be specified independently for RAM0 and RAM1.	Can transition to module stop state
Error check function	—	• Parity error detection • A non-maskable or maskable interrupt is generated when an error occurs

Note: 1. The number of cycles doubles when access crosses the 8-byte boundary.

Table 2.80 Comparison of RAM Registers

Register	Bit	RX210	RX261
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.31 Flash Memory

Table 2.81 shows a Comparative Overview of Flash Memory and Table 2.82 shows a Comparison of Flash Memory Registers.

Table 2.81 Comparative Overview of Flash Memory

Item	RX210	RX261 (FLASH)
Memory size	• User area: Maximum of 1 MB • Data area: 8 KB • User boot area: 16 KB	• User area: Maximum of 512 KB • Data area: 8 KB • Extra area: Stores start-up area information, access window information, and unique IDs
Addresses	User area • Products with memory size of 1 MB — FFF0 0000h to FFFF FFFFh • Products with memory size of 768 KB — FFF4 0000h to FFFF FFFFh • Products with memory size of 512 KB — FFF8 0000h to FFFF FFFFh • Products with memory size of 384 KB — FFFA 0000h to FFFF FFFFh • Products with memory size of 256 KB — FFFC 0000h to FFFF FFFFh • Products with memory size of 128 KB — FFFE 0000h to FFFF FFFFh • Products with memory size of 96 KB — FFFE 8000h to FFFF FFFFh • Products with memory size of 64 KB — FFFF 0000h to FFFF FFFFh Data area • 8 KB — 0010 0000h to 0010 1FFFh	User area • Products with memory size of 512 KB — FFF8 0000h to FFFF FFFFh • Products with memory size of 384 KB — FFFA 0000h to FFFF FFFFh • Products with memory size of 256 KB — FFFC 0000h to FFFF FFFFh Data area • 8 KB — 0010 0000h to 0010 1FFFh
Operating clock	• FCLK: 4 to 32 MHz (in ROM P/E mode and E2 DataFlash P/E mode) Maximum of 32 MHz (in E2 DataFlash read mode)	• FCLK: 1 to 64 MHz (in ROM P/E mode and E2 DataFlash P/E mode) Maximum of 64 MHz (in E2 DataFlash read mode) • HOCO clock: 24 MHz, 32 MHz, 48 MHz, or 64 MHz (in ROM P/E mode and E2 DataFlash P/E mode)

Item	RX210	RX261 (FLASH)
FCU commands (RX210) Software commands (RX261)	• The following software commands are implemented: — P/E normal mode transition, status read mode transition, lock bit read mode transition, peripheral clock notification, programming, block erase, P/E suspend, P/E resume, status register clear, lock bit read 2/blank check, lock bit programming	• The following software commands are implemented: — Programming, blank check, block erase, and all-block erase • The following commands are implemented for extra area programming: — Start-up area information program, access window protection, and access window information program
Values after erase	• ROM: FFh • E2 DataFlash: Undefined	• ROM: FFh • E2 DataFlash: FFh
Interrupts	An interrupt (FRDYI) is generated at completion of an FCU command.	An interrupt (FRDYI) is generated at completion of software command processing or forced stop processing.

Item	RX210	RX261 (FLASH)
On-board programming	• Reprogramming in boot mode — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area can also be programmed. • Reprogramming in user boot mode — The user-specific boot program can be programmed. • Reprogramming using the ROM reprogramming routine in the user program — ROM and E2 data flash can be programmed without resetting the system.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used in asynchronous mode. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Boot mode (USB interface) — Channel 0 of the USB 2.0 function (USB0) module is used. — The user area and data area can be programmed. — Flash memory can be rewritten in self-powered or bus-powered mode. — The product can connect to a personal computer using only a USB cable. • Self-programming (single-chip mode) — The user area and data area can be programmed by using a flash programming routine in a user program.

Item		RX210	RX261 (FLASH)
Off-board programming		The user area and user boot area can be programmed by using the PROM programmer.	—
Protection	Start-up program protection function	—	A function used to safely program blocks 0 to 7
	Area protection	—	During self-programming, this function enables programming only of specified blocks in the user area, while preventing programming of the other blocks.
	ID code protection	—	• Connections to serial programmers can be permitted or denied based on ID code in boot mode. • Connections to an on-chip debugging emulator can be controlled using ID codes
	Software-controlled protection	The FENTRYR.FENTRY0 bit, FENTRYR.FENTRY1 bit, FENTRYR.FENTRYD bit, FWEPROR.FLWE[1:0] bits, lock bit, DFLRE0 register, and DFLWE0 register can be used to prevent unintentional programming.	DFLCTL.DFLEN bit FENTRYR.FENTRY0 bit, and FENTRYR.FENTRYD bit can be used to prevent unintentional programming.
	Command lock function	If abnormal operation is detected during programming or erasure, further programming or erasure is disabled.	—
Background operation (BGO) function		• Programs in the ROM area can run while the E2 DataFlash is being programmed or erased. • The CPU can run programs in an area other than the ROM/E2 DataFlash while the ROM is being programmed or erased.	Programs on the ROM can run while the E2 DataFlash is being rewritten.

Table 2.82 Comparison of Flash Memory Registers

Register	Bit	RX210	RX261 (FLASH)
DFLCTL	—	—	E2 DataFlash control register
FENTRYR	FENTRY0	ROM P/E mode entry bit 0 0: 64, 96, 128, 256, 384, or 512 Kbytes (area 0) of ROM are in ROM read mode. 1: 64, 96, 128, 256, 384, or 512 Kbytes (area 0) of ROM are in ROM P/E mode.	ROM P/E mode entry bit 0 0: ROM is in read mode. 1: ROM can be placed in P/E mode.
	FENTRY1	ROM P/E mode entry bit 1	—
MEMWAITR	—	—	Memory wait cycle setting register
FPR	—	—	Protection unlock register

Register	Bit	RX210	RX261 (FLASH)
FPSR	—	—	Protection unlock status register
FPMCR	—	—	Flash P/E mode control register
FISR	—	—	Flash initial setting register
FRESETR	—	Flash reset register FRESETR is a 16-bit register.	Flash reset register FRESETR is an 8-bit register.
	FRKEY[7:0]	Key code	—
FASR	—	—	Flash area select register
FCR	—	—	Flash control register
FEXCR	—	—	Flash extra area control register
FSARH	—	—	Flash processing start address register H
FSARL	—	—	Flash processing start address register L
FEARH	—	—	Flash processing end address register H
FEARL	—	—	Flash processing end address register L
FWBn	—	—	Flash write buffer register n (n = 0 to 3)
FSTATR0	ERSERR (RX210) ERERR (RX261)	Erasure error bit (b5)	Erasure error bit (b0)
	PRGERR	Programming error bit (b4)	Programming error bit (b1)
	BCERR	—	Blank check error flag
	ILGLERR	Illegal command error bit (b6)	Illegal command error flag (b4)
	EILGLERR	—	Extra area illegal command error flag
	PRGSPD	Programming suspend status bit	—
	ERSSPD	Erasure suspend status bit	—
	SUSRDY	Suspend ready bit	—
	FRDY	Flash ready bit	—
FSTATR1	FRDY	—	Flash ready flag
	EXRDY	—	Extra area ready flag
	FLOCKST	Lock bit status bit	—
	FCUERR	FCU error bit	—
	The value after a reset differs.		
FEAMH	—	—	Flash error address monitor register H
FEAML	—	—	Flash error address monitor register L
FSCMR	—	—	Flash start-up setting monitor register

Register	Bit	RX210	RX261 (FLASH)
FAWSMR	—	—	Flash access window start address monitor register
FAWEMR	—	—	Flash access window end address monitor register
UIDRn	—	—	Unique ID register n (n = 0 to 3)
FWEPROR	—	Flash write erase protection register	—
FMODR	—	Flash mode register	—
FASTAT	—	Flash access status register	—
FAEINT	—	Flash access error interrupt enable register	—
FCURAME	—	FCU RAM enable register	—
FRDYIE	—	Flash ready interrupt enable register	—
FPROTR	—	Flash protection register	—
FCMDR	—	FCU command register	—
FCPSR	—	FCU processing switching register	—
FPESTAT	—	Flash P/E status register	—
PCKAR	—	Peripheral clock notification register	—
DFLRE0	—	E2 DataFlash read enable register 0	—
DFLWE0	—	E2 DataFlash programming/erasure enable register 0	—
DFLBCCNT	—	E2 DataFlash blank check control register	—
DFLBCSTAT	—	E2 DataFlash blank check status register	—

2.32 Packages

As shown in Table 2.83, there are differences in the package drawing codes and availability of some package types. Please bear this in mind at the board design stage.

Table 2.83 Packages

	RENESAS Code			
	RX210			**RX261**
Package Type	**Chip Version A**	**Chip Version B**	**Chip Version C**	**—**
145-pin TFLGA	×	○	×	×
144-Pin LQFP	×	○	×	×
100-pin LFQFP	×	×	×	○
100-pin TFLGA	PTLG0100JA-A	PTLG0100JA-A PTLG0100KA-A	PTLG0100JA-A	×
100-Pin LQFP	○	○	○	×
80-pin LFQFP	×	×	×	○
80-Pin LQFP	PLQP0080KB-A	PLQP0080KB-A PLQP0080JA-A	PLQP0080KB-A PLQP0080JA-A	×
69-pin WLBGA	×	○	×	×
64-pin LFQFP	×	×	×	○
64-pin TFLGA	×	○	×	×
64-Pin LQFP	PLQP0064KB-A	PLQP0064KB-A PLQP0064GA-A	PLQP0064KB-A PLQP0064GA-A	×
48-pin LFQFP	×	×	×	○
48-pin HWQFN	×	×	×	○
48-Pin LQFP	×	○	×	×

○: Package available (RENESAS code omitted), ×: Package not available

3. Comparison of Pin Functions

The following presents a comparison of pin functions, and compares the pins used for the power supply, clocks, and system control. **Blue text** indicates pin functions that are included in only one of the MCU groups, and **red text** indicates pin functions that are present in both groups but differ in some respect. Pin functions whose specifications do not differ between the groups are shown in **black text**.

3.1 100-Pin Package

Table 3.1 shows a Comparison of 100-Pin Package Pin Functions.

Table 3.1 Comparison of 100-Pin Package Pin Functions

100-Pin	RX210 (100-Pin LQFP)	RX261 (100-Pin LFQFP)
1	VREFH	P06*3
2	P03/DA0	P03*3/DA0
3	VREFL	P04*3
4	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#	PJ3/GTIOC6B/GTIOC6B#/CTS6#/RTS6#/SS6#
5	VCL	VCL
6	PJ1/MTIOC3A	PJ1/GTIOC6A/GTIOC6A#/GTCPPO0
7	MD/FINED	MD/FINED/PG7
8	XCIN	XCIN/PH7
9	XCOUT	XCOUT/EXCIN/PH6
10	RES#	RES#
11	XTAL/P37	XTAL/P37/IRQ4
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/IRQ2
14	VCC	VCC
15	P35/NMI	UPSEL/P35/NMI
16	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	P34/GTIOC3A/GTIOC3A#/GTIU/TMCI3/SCK6/IRQ4
17	P33/MTIOC0D/TMRI3/POE3#/RXD6/SMISO6/SSCL6/IRQ3-DS	P33/GTIOC1B/GTIOC7B/GTIOC1B#/GTIOC7B#/TMRI3/RXD6/SMISO6/SSCL6/CRX0*2/IRQ3
18	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/IRQ2-DS/RTCOUT/RTCIC2	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/CTX0*2/USB0_VBUSEN*2/TS0/IRQ2
19	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/IRQ1-DS/RTCIC1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
20	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/RTCIC0	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
21	P27/CS3#/MTIOC2B/TMCI3/SCK1	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
22	P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
23	P25/CS1#/MTIOC4C/MTCLKB/ADTRG0#	P25/GTIOC1B/GTIOC6A/GTIOC1B#/GTIOC6A#/GTETRGB/ADTRG0#
24	P24/CS0#/MTIOC4A/MTCLKA/TMRI1	P24/GTIOC1A/GTIOC6B/GTIOC1A#/GTIOC6B#/GTETRGA/TMRI1/USB0_VBUSEN*2
25	P23/MTIOC3D/MTCLKD/CTS0#/RTS0#/SS0#	P23/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/GTETRGD/CTS000#/RTS000#/SS000#/DE000
26	P22/MTIOC3B/MTCLKC/TMO0/SCK0	P22/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/GTETRGC/TMO0/SCK000/TXDB000/USB0_OVRCURB*2

100-Pin	RX210 (100-Pin LQFP)	RX261 (100-Pin LFQFP)
27	P21/MTIOC1B/TMCI0/RXD0/SMISO0/SSCL0	P21/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/ TMCI0/RXD000/SMISO000/SSCL000/ USB0_EXICEN*2
28	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0	P20/GTIOC2B/GTIOC4A/GTIOC2B#/GTIOC4A#/ TMRI0/TXD000/TXDA000/SMOSI000/SSDA000/ USB0_ID*2
29	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/ MISOA/SDA-DS/IRQ7	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
30	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL-DS/IRQ6/RTCOUT/ ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/IRQ5	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
32	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/IRQ4	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
33	P13/MTIOC0B/TMO3/SDA/IRQ3	P13/GTIOC3B/GTIOC7A/GTIOC3B#/GTIOC7A#/ GTIV/TMO3/SDA0/IRQ3
34	P12/TMCI1/SCL/IRQ2	P12/TMCI1/SCL0/IRQ2
35	PH3/TMCI0	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
36	PH2/TMRI0/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/ TMRI0*1/USB0_DM*2/TS8*1/IRQ1*1
37	PH1/TMO0/IRQ0	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/ IRQ0*1
38	PH0/CACREF	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
39	P55/WAIT#/MTIOC4D/TMO3	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/ TMO3/CRX0*2/TS11
40	P54/ALE/MTIOC4B/TMCI1	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*2/TS12
41	BCLK/P53	P53/PMC0
42	P52/RD#	P52
43	P51/WR1#/BC1#/WAIT#	P51/PMC0
44	P50/WR0#/WR#	P50
45	PC7/A23/CS0#/MTIOC3A/TMO2/MTCLKB/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
46	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/ RXD8/SMISO8/SSCL8/MOSIA	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14
47	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/SCK8/RSPCKA	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP

100-Pin	RX210 (100-Pin LQFP)	RX261 (100-Pin LFQFP)
49	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/SMOSI5/SSDA5/PMC0/TS16
50	PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/RXD5/SMISO5/SSCL5/SSLA3/TS17
51	PC1/A17/MTIOC3A/SCK5/SSLA2	PC1/GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/SCK5/SSLA2
52	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/SSLA1	PC0/GTIOC6B/GTIOC6B#/GTETRGC/CTS5#/RTS5#/SS5#/SSLA1
53	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9	PB7/GTIOC0A/GTIOC7B/GTIOC0A#/GTIOC7B#/TXD009/TXDA009/SMOSI009/SSDA009/TS18
54	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9	PB6/GTIOC0B/GTIOC7A/GTIOC0B#/GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
55	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE1#/SCK9	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/USB0_VBUS*2/TS20
56	PB4/A12/CTS9#/RTS9#/SS9#	PB4/GTIOC6A/GTIOC6A#/CTS009#/RTS009#/SS009#/DE009/TS21
57	PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
58	PB2/A10/CTS6#/RTS6#/SS6#	PB2/GTIOC3A/GTIOC3A#/GTETRGC/CTS6#/RTS6#/SS6#/TS23
59	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
60	VCC	VCC
61	PB0/A8/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
62	VSS	VSS
63	PA7/A7/MISOA	PA7/GTIOC5B/GTIOC5B#/MISOA
64	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/SS5#/MOSIA/TS26
65	PA5/A5/RSPCKA	PA5/GTIOC4B/GTIOC4B#/RSPCKA/TS27
66	PA4/A4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
67	PA3/A3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/IRQ6-DS/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
68	PA2/A2/RXD5/SMISO5/SSCL5/SSLA3	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
69	PA1/A1/MTIOC0B/MTCLKC/SCK5/SSLA2/CVREFA	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/SCK5/SSLA2/TS31
70	PA0/A0/BC0#/MTIOC4A/SSLA1/CACREF	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/GTOVUP/CACREF/SSLA1/TS32
71	PE7/D15[A15/D15]/IRQ7/AN015	PE7/IRQ7/AN023
72	PE6/D14[A14/D14]/IRQ6/AN014	PE6/IRQ6/AN022

100-Pin	RX210 (100-Pin LQFP)	RX261 (100-Pin LFQFP)
73	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/AN013	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/IRQ5/AN021/CMPOB0
74	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN012/CMPA2	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/GTOWLO/TS33/AN020/CMPA2
75	PE3/D11[A11/D11]/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AN011/CMPA1	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/TS34/AN019
76	PE2/D10[A10/D10]/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7-DS/AN010/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
77	PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN009/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/AN017/CMPB0
78	PE0/D8[A8/D8]/SCK12/AN008	PE0/SCK12/AN016
79	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7	PD7/IRQ7/AN031
80	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6	PD6/IRQ6/AN030
81	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5	PD5/IRQ5/AN029
82	PD4/D4[A4/D4]/POE3#/IRQ4	PD4/IRQ4/AN028
83	PD3/D3[A3/D3]/POE8#/IRQ3	PD3/IRQ3/AN027
84	PD2/D2[A2/D2]/MTIOC4D/IRQ2	PD2/GTIOC2B/GTIOC2B#/SCK6/CRX0*2/IRQ2/AN026
85	PD1/D1[A1/D1]/MTIOC4B/IRQ1	PD1/GTIOC2A/GTIOC2A#/RXD6/SMISO6/SSCL6/CTX0*2/IRQ1/AN025
86	PD0/D0[A0/D0]/IRQ0	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
87	P47/AN007	P47*3/AN007
88	P46/AN006	P46*3/AN006
89	P45/AN005	P45*3/AN005
90	P44/AN004	P44*3/AN004
91	P43/AN003	P43*3/AN003
92	P42/AN002	P42*3/AN002
93	P41/AN001	P41*3/AN001
94	VREFL0	VREFL0/PJ7*3
95	P40/AN000	P40*3/AN000
96	VREFH0	VREFH0/PJ6*3
97	AVCC0	AVCC0
98	P07/ADTRG0#	P07*3/ADTRG0#
99	AVSS0	AVSS0
100	P05/DA1	P05*3/DA1

Notes: 1. Unavailable in RX261 Group products.
2. Unavailable in RX260 Group products.
3. The power supply for the I/O buffer for these pins is AVCC0.

3.2 80-Pin Package

Table 3.2 shows a Comparison of 80-Pin Package Pin Functions.

Table 3.2 Comparison of 80-Pin Package Pin Functions

80-Pin	RX210 (80-Pin LQFP)	RX261 (80-Pin LFQFP)
1	VREFH	P06*3
2	P03/DA0	P03*3/DA0
3	VREFL	P04*3
4	VCL	VCL
5	PJ1/MTIOC3A	PJ1/GTIOC6A/GTIOC6A#/GTCPPO0
6	MD/FINED	MD/FINED/PG7
7	XCIN	XCIN/PH7
8	XCOUT	XCOUT/EXCIN/PH6
9	RES#	RES#
10	XTAL/P37	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/IRQ2
13	VCC	VCC
14	P35/NMI	UPSEL/P35/NMI
15	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4	P34/GTIOC3A/GTIOC3A#/GTIU/TMCI3/SCK6/IRQ4
16	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/IRQ2-DS/RTCOUT/RTCIC2	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/CTX0*2/USB0_VBUSEN*2/TS0/IRQ2
17	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/IRQ1-DS/RTCIC1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
18	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/RTCIC0	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
19	P27/MTIOC2B/TMCI3/SCK1	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
20	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
21	P21/MTIOC1B/TMCI0/RXD0/SSCL0	P21/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/TMCI0/RXD000/SMISO000/SSCL000/USB0_EXICEN*2
22	P20/MTIOC1A/TMRI0/TXD0/SSDA0	P20/GTIOC2B/GTIOC4A/GTIOC2B#/GTIOC4A#/TMRI0/TXD000/TXDA000/SMOSI000/SSDA000/USB0_ID*2
23	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA-DS/IRQ7	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
24	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL-DS/IRQ6/RTCOUT/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/USB0_VBUS*2/USB0_VBUSEN*2/USB0_OVRCURB*2/IRQ6/ADTRG0#
25	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/IRQ5	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/CRX0*2/TS5/IRQ5
26	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/IRQ4	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4

80-Pin	RX210 (80-Pin LQFP)	RX261 (80-Pin LFQFP)
27	P13/MTIOC0B/TMO3/SDA/IRQ3	P13/GTIOC3B/GTIOC7A/GTIOC3B#/GTIOC7A#/GTIV/TMO3/SDA0/IRQ3
28	P12/TMCI1/SCL/IRQ2	P12/TMCI1/SCL0/IRQ2
29	PH3/TMCI0	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
30	PH2/TMRI0/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/TMRI0*1/USB0_DM*2/TS8*1/IRQ1*1
31	PH1/TMO0/IRQ0	PH1*1/GTIOC0B*1/GTIOC0B#*1/GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/IRQ0*1
32	PH0/CACREF	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/TS10
33	P55/MTIOC4D/TMO3	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/TMO3/CRX0*2/TS11
34	P54/MTIOC4B/TMCI1	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*2/TS12
35	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/GTCPPO0/TMO2/LPTO/CACREF/TXD008/TXDA008/SMOSI008/SSDA008/MISOA/TS13
36	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/SSCL8/MOSIA	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/RXD008/SMISO008/SSCL008/MOSIA/USB0_EXICEN*2/TS14
37	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
38	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/GTETRGC/GTIU/GTOULO/TMCI1/SCK5/CTS008#/RTS008#/SS008#/DE008/SSLA0/PMC0/TSCAP
39	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/SMOSI5/SSDA5/PMC0/TS16
40	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/RXD5/SMISO5/SSCL5/SSLA3/TS17
41	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9	PB7/PC1*4/GTIOC0A/GTIOC7B/GTIOC0A#/GTIOC7B#/TXD009/TXDA009/SMOSI009/SSDA009/TS18
42	PB6/MTIOC3D/RXD9/SMISO9/SSCL9	PB6/PC0*4/GTIOC0B/GTIOC7A/GTIOC0B#/GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
43	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/SCK9	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/USB0_VBUS*2/TS20
44	PB4/CTS9#/RTS9#/SS9#	PB4/GTIOC6A/GTIOC6A#/CTS009#/RTS009#/SS009#/DE009/TS21
45	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
46	PB2/CTS6#/RTS6#/SS6#	PB2/GTIOC3A/GTIOC3A#/GTETRGC/CTS6#/RTS6#/SS6#/TS23
47	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/IRQ4-DS	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
48	VCC	VCC

80-Pin	RX210 (80-Pin LQFP)	RX261 (80-Pin LFQFP)
49	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
50	VSS	VSS
51	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/SS5#/MOSIA/TS26
52	PA5/RSPCKA	PA5/GTIOC4B/GTIOC4B#/RSPCKA/TS27
53	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
54	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/IRQ6-DS/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
55	PA2/RXD5/SMISO5/SSCL5/SSLA3	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
56	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/CVREFA	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/SCK5/SSLA2/TS31
57	PA0/MTIOC4A/SSLA1/CACREF	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/GTOVUP/CACREF/SSLA1/TS32
58	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/IRQ5/AN021/CMPOB0
59	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/GTOWLO/TS33/AN020/CMPA2
60	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AN011/CMPA1	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/TS34/AN019
61	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7-DS/AN010/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
62	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN009/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/AN017/CMPB0
63	PE0/SCK12/AN008	PE0/SCK12/AN016
64	PD2/MTIOC4D/IRQ2	PD2/GTIOC2B/GTIOC2B#/SCK6/CRX0*2/IRQ2/AN026
65	PD1/MTIOC4B/IRQ1	PD1/GTIOC2A/GTIOC2A#/RXD6/SMISO6/SSCL6/CTX0*2/IRQ1/AN025
66	PD0/IRQ0	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
67	P47/AN007	P47*3/AN007
68	P46/AN006	P46*3/AN006
69	P45/AN005	P45*3/AN005
70	P44/AN004	P44*3/AN004
71	P43/AN003	P43*3/AN003
72	P42/AN002	P42*3/AN002
73	P41/AN001	P41*3/AN001
74	VREFL0	VREFL0/PJ7*3
75	P40/AN000	P40*3/AN000
76	VREFH0	VREFH0/PJ6*3
77	AVCC0	AVCC0

80-Pin	RX210 (80-Pin LQFP)	RX261 (80-Pin LFQFP)
78	P07/ADTRG0#	P07*3/ADTRG0#
79	AVSS0	AVSS0
80	P05/DA1	P05*3/DA1

Notes: 1. Unavailable in RX261 Group products.
2. Unavailable in RX260 Group products.
3. The power supply for the I/O buffer for these pins is AVCC0.
4. PC0 and PC1 are available only when the port switching function is selected.

3.3 64-Pin Package

Table 3.3 shows a Comparison of 64-Pin Package Pin Functions.

Table 3.3 Comparison of 64-Pin Package Pin Functions

64-Pin	RX210 (64-Pin LQFP)	RX261 (64-Pin LFQFP)
1	P03/DA0	P03*3/DA0
2	VCL	VCL
3	MD/FINED	MD/FINED/PG7
4	XCIN	XCIN/PH7
5	XCOUT	XCOUT/EXCIN/PH6
6	RES#	RES#
7	XTAL/P37	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/IRQ2
10	VCC	VCC
11	P35/NMI	UPSEL/P35/NMI
12	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/ IRQ2-DS/RTCOUT/RTCIC2	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/ SSDA6/CTX0*2/USB0_VBUSEN*2/TS0/IRQ2
13	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS/RTCIC1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
14	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/ SSCL1/IRQ0-DS/RTCIC0	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
15	P27/MTIOC2B/TMCI3/SCK1	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/ MISOA/SDA-DS/IRQ7	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
18	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL-DS/IRQ6/RTCOUT/ ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/IRQ5	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
20	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/IRQ4	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
21	PH3/TMCI0	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
22	PH2/TMRI0/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/ TMRI0*1/USB0_DM*2/TS8*1/IRQ1*1
23	PH1/TMO0/IRQ0	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/ IRQ0*1
24	PH0/CACREF	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
25	P55/MTIOC4D/TMO3	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/ TMO3/CRX0*2/TS11

64-Pin	RX210 (64-Pin LQFP)	RX261 (64-Pin LFQFP)
26	P54/MTIOC4B/TMCI1	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*2/ TS12
27	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/SMOSI8/ SSDA8/MISOA/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
28	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/ SSCL8/MOSIA	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14
29	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/ CTS8#/RTS8#/SS8#/SSLA0	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP
31	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/ SMOSI5/SSDA5/PMC0/TS16
32	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/ RXD5/SMISO5/SSCL5/SSLA3/TS17
33	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9	PB7/PC1*4/GTIOC0A/GTIOC7B/GTIOC0A#/ GTIOC7B#/TXD009/TXDA009/SMOSI009/ SSDA009/TS18
34	PB6/MTIOC3D/RXD9/SMISO9/SSCL9	PB6/PC0*4/GTIOC0B/GTIOC7A/GTIOC0B#/ GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/SCK9	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/ GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/ USB0_VBUS*2/TS20
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/ GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/ TMO0/LPTO/SCK6/PMC0/TS22
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/ SSDA6/IRQ4-DS	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/ TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/ CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/ GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/ TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/ RTS5#/SS5#/MOSIA	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/ SS5#/MOSIA/TS26
42	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
43	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/ IRQ6-DS/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1
44	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/CVREFA	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/ SCK5/SSLA2/TS31

64-Pin	RX210 (64-Pin LQFP)	RX261 (64-Pin LFQFP)
45	PA0/MTIOC4A/SSLA1/CACREF	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/GTOVUP/CACREF/SSLA1/TS32
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/IRQ5/AN021/CMPOB0
47	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/GTOWLO/TS33/AN020/CMPA2
48	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AN011/CMPA1	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/TS34/AN019
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7-DS/AN010/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN009/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/AN017/CMPB0
51	PE0/SCK12/AN008	PE0/SCK12/AN016
52	VREFL	P47*3/AN007
53	P46/AN006	P46*3/AN006
54	VREFH	P45*3/AN005
55	P44/AN004	P44*3/AN004
56	P43/AN003	P43*3/AN003
57	P42/AN002	P42*3/AN002
58	P41/AN001	P41*3/AN001
59	VREFL0	VREFL0/PJ7*3
60	P40/AN000	P40*3/AN000
61	VREFH0	VREFH0/PJ6*3
62	AVCC0	AVCC0
63	P05/DA1	P05*3/DA1
64	AVSS0	AVSS0

Notes: 1. Unavailable in RX261 Group products.
2. Unavailable in RX260 Group products.
3. The power supply for the I/O buffer for these pins is AVCC0.
4. PC0 and PC1 are available only when the port switching function is selected.

3.4 48-Pin Package

Table 3.4 shows a Comparison of 48-Pin Package Pin Functions.

Table 3.4 Comparison of 48-Pin Package Pin Functions

48-Pin	RX210 (48-Pin LQFP)	RX261 (48-Pin LFQFP, HWQFN)
1	VCL	VCL
2	MD/FINED	MD/FINED/PG7
3	RES#	RES#
4	XTAL/P37	XTAL/P37/IRQ4
5	VSS	VSS
6	EXTAL/P36	EXTAL/P36/IRQ2
7	VCC	VCC
8	P35/NMI	UPSEL/P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ CTS1#/RTS1#/SS1#/TS1/IRQ1
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/ SSCL1/IRQ0-DS	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RXD1/SMISO1/SSCL1/TS2/IRQ0
11	P27/MTIOC2B/TMCI3/SCK1	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/ MISOA/SDA-DS/IRQ7	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
14	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL-DS/IRQ6/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/ USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
15	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/IRQ5	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
16	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/IRQ4	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
17	PH3/TMCI0	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
18	PH2/TMRI0/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/ TMRI0*1/USB0_DM*2/TS8*1/IRQ1*1
19	PH1/TMO0/IRQ0	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/ IRQ0*1
20	PH0/CACREF	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
21	PC7/MTIOC3A/TMO2/MTCLKB/TXD8/SMOSI8/ SSDA8/MISOA/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
22	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/ SSCL8/MOSIA	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14
23	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15

48-Pin	RX210 (48-Pin LQFP)	RX261 (48-Pin LFQFP, HWQFN)
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/ CTS8#/RTS8#/SS8#/SSLA0	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP
25	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#	PB5/PC3*4/GTIOC4B/GTIOC5A/GTIOC4B#/ GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/ USB0_VBUS*2/TS20
26	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6	PB3/PC2*4/GTIOC1A/GTIOC3A/GTIOC1A#/ GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/ GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
27	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/ SSDA6/IRQ4-DS	PB1/PC1*4/GTIOC1B/GTIOC2B/GTIOC1B#/ GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/ GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/ TS24/IRQ4/CMPOB1
28	VCC	VCC
29	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA	PB0/PC0*4/GTIOC0B/GTIOC2A/GTIOC0B#/ GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/ RSPCKA/TS25
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/ RTS5#/SS5#/MOSIA	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/ SS5#/MOSIA/TS26
32	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/IRQ5-DS/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
33	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/ IRQ6-DS/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1
34	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/CVREFA	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/ SCK5/SSLA2/TS31
35	PE4/MTIOC4D/MTIOC1A/AN012/CMPA2	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
36	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/AN011/ CMPA1	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/TS34/ AN019
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/ IRQ7-DS/AN010/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SSDA12/ AN009/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SSDA12/TXDX12/SIOX12/AN017/CMPB0
39	VREFL	P47*3/AN007
40	P46/AN006	P46*3/AN006
41	VREFH	P45*3/AN005
42	P42/AN002	P42*3/AN002
43	P41/AN001	P41*3/AN001
44	VREFL0	VREFL0/PJ7*3
45	P40/AN000	P40*3/AN000
46	VREFH0	VREFH0/PJ6*3
47	AVCC0	AVCC0

48-Pin	RX210 (48-Pin LQFP)	RX261 (48-Pin LFQFP, HWQFN)
48	AVSS0	AVSS0

Notes: 1. Unavailable in RX261 Group products.
2. Unavailable in RX260 Group products.
3. The power supply for the I/O buffer for these pins is AVCC0.
4. PC0 to PC3 are available only when the port switching function is selected.

4. Important Information when Migrating Between MCUs

Some of the software that runs on the RX210 Group is compatible with the RX261 Group. However, due to differences in aspects such as operation timing and electrical characteristics, you must evaluate your circumstances thoroughly.

The following explains software-related matters to consider in relation to function settings that differ between the RX261 Group and RX210 Group.

For differences between modules and functions, refer to section 2, “Comparative Overview of Specifications”.

For details, refer to the User’s Manual: Hardware document listed in section 5, “Reference Documents”.

4.1 Considerations for Functional Design

4.1.1 VCL Pin (External Capacitance)

When connecting a smoothing capacitor to the RX261 Group VCL pin to stabilize the internal power supply, use a capacitance of 4.7 µF.

4.1.2 User Boot Mode

The RX210 Group products have UB code A, UB code B, and user boot mode while the RX261 products do not.

The RX261 Group products have start-up program protection that allows programming or erasure of a user area in flash memory by using any interface in place of user boot mode. For details, refer to section 46.5, “Start-Up Program Protection” in the RX261 Group User’s Manual: Hardware listed in section 5, “Reference Documents”.

4.1.3 Clock Frequency Settings

The RX261 Group and RX210 Group have different restrictions in relation to clock frequency settings. For details, refer to Table 4.1.

Table 4.1 Comparison of Restrictions on Clock Frequency Settings

Item	RX210	RX261
Restrictions on clock frequency settings	ICLK ≥ BCLK	PCLKA ≥ PCLKB PCLKB ≥ CANFDCLK (when CANFD is used) PCLKB ≥ CANFDMCLK (when CANFD is used)
Restrictions on clock frequency ratio	—	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKB = 2:1 (when CANFD is used)

4.1.4 PLL Circuit

The multiplication factor of the PLL circuit is within a range from 8 to 25× in the RX210 Group, and within a range from 4 to 15.5× (in increments of 0.5) in the RX261 Group. When using the PLL circuit, change the setting value of the PLLCR.STC bit to an appropriate value.

4.1.5 Exception Vector Table

The vector table is allocated to a fixed address range in the RX210 Group. In the RX261 Group, the vector table can be allocated in any area in which the value set in the exception table register (EXTB) is used as the starting address.

4.1.6 Restrictions on Compare Function

The compare function of the RX261 Group 12-bit A/D converter has the following restrictions.

1. The compare function cannot be used with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD and ADDBLDR registers.)
2. When using matching or unmatching event output, specify single scan mode.
3. Window B operation is disabled when temperature sensor or internal reference voltage is selected for window A.
4. Window A operation is disabled when temperature sensor or internal reference voltage is selected for window B.
5. The same channel cannot be set for window A and window B.
6. When using the buffer function, specify single scan mode. (Concurrent use of double trigger mode is also prohibited.)
7. Make sure that the high-side reference value is equal to or larger than the low-side reference value.

4.1.7 MOSCWTCR Register

The RX210 Group products count the main clock, and the RX261 Group products count the LOCO clock.

4.1.8 Noise Cancellation for I²C Bus Interface

The RX210 Group products incorporate analog noise filters in the SCL and SDA lines. The RX261 Group products do not incorporate analog noise filters.

4.1.9 Port Direction Register (PRD) Initialization

PDR register initialization differs between RX261 Group products even when they have the same pin count.

4.1.10 12-Bit A/D Converter Scan Conversion Time

The scan conversion time differs between the RX261 Group and the RX210 Group. The scan conversion time (t_{SCAN}) in single scan mode for each group is calculated as follows, where n is the number of selected channels. For details, refer to the description of the analog input sampling and scan conversion time of the 12-bit A/D converter in the User's Manual: Hardware documents for the RX261 Group and RX210 Group listed in section 5, "Reference Documents".

RX210: $t_{SCAN} = t_D + t_{SH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

RX261: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_D …Start-of-scanning-delay time
t_{SH} …Channel-dedicated sample-and-hold circuits sampling time
t_{DIS} …Disconnection detection assist processing time
t_{DIAG} …Self-diagnosis A/D conversion processing time
t_{CONV} …A/D conversion processing time
t_{ED} …End-of-scanning-delay time

4.1.11 Notes on High-Speed Operating Mode

The maximum operating frequency of the FLASH read time in high-speed operating mode differs between the RX210 Group and the RX261 Group. For details, refer to Table 4.2, “Comparison of Maximum Operating Frequency of FLASH Read Time in High-Speed Operating Mode”.

Table 4.2 Comparison of Maximum Operating Frequency of FLASH Read Time in High-Speed Operating Mode

Item	RX210	RX261
ICLK	50 MHz	64 MHz
FCLK	32 MHz	64 MHz
PCLKD	50 MHz	64 MHz
PCLKB	32 MHz	32 MHz
PCLKA	—	64 MHz
BCLK	25 MHz	—

4.1.12 RTC Control Register 2 (RCR2)

The registers that can be reset by setting the RTC software reset bit differ between the RX210 Group and the RX261 Group.

4.1.13 A/D Disconnection Detection Control Register (ADDISCR)

For the RX210 Group, any set value of the ADNDIS[3:0] bits other than 0000b is valid as the number of precharge/discharge states. For the RX261 Group, setting the ADNDIS[3:0] bits to 0001b is prohibited.

5. Reference Documents

User's Manual: Hardware

RX210 Group User's Manual: Hardware Rev.1.50 (R01UH0905EJ0150)
(The latest version is available from the Renesas Electronics website.)

RX260/RX261 Group User's Manual: Hardware Rev.1.00 (R01UH1045EJ0100)
(The latest version is available from the Renesas Electronics website.)

Technical Updates/Technical News

(The latest information is available from the Renesas Electronics website.)

Related Technical Updates

This application note contains information from the following technical updates:

- TN-RX*-A087A/E
- TN-RX*-A097A/E
- TN-RX*-A094A/E
- TN-RX*-A096A/E
- TN-RX*-A099A/E
- TN-RX*-A107A/E
- TN-RX*-A118A/E
- TN-RX*-A035B/E
- TN-RX*-A130B/E
- TN-RX*-A138A/E
- TN-RX*-A141A/E
- TN-RX*-A147A/E
- TN-RX*-A151A/E
- TN-RX*-A177A/E
- TN-RX*-A188A/E
- TN-RX*-A193A/E
- TN-RX*-A0147B/E
- TN-RX*-A0231A/E
- TN-RX*-A0224B/E
- TN-RX*-A0239B/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug. 7, 2024	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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